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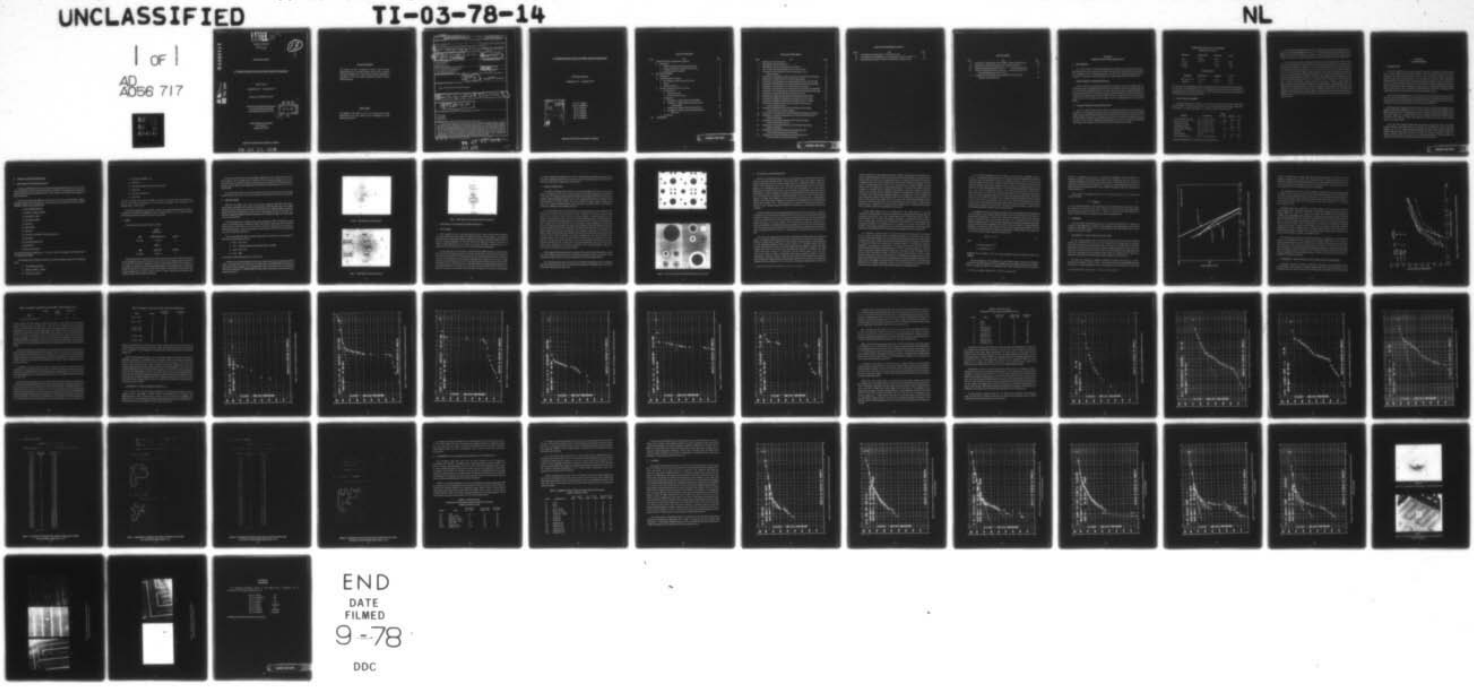

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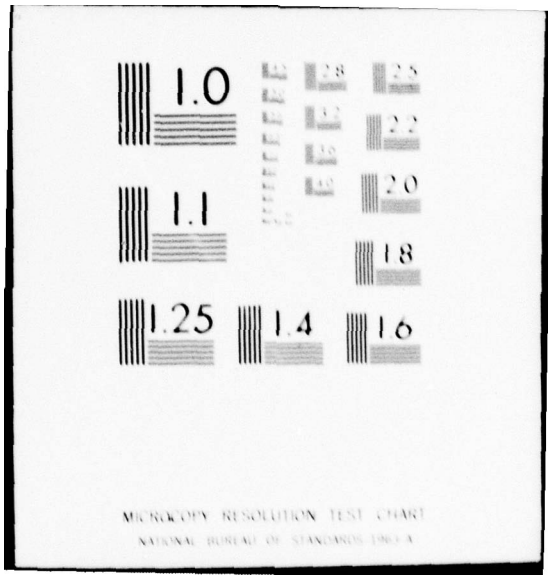
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Report No. 03-78-14

Fifth Quarterly Report

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Fort Monmouth, New Jersey 07703

Texas Instruments Incorporated
P.O. Box 5012
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(10) Gilbert L. Varnell, John L. Bartelt, Claude D. Winborn, Ronald A. Williamson, George A. Brown, Terry L. Brewer, Roger A. Robbins

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Continuity and integrity of electron beam resist films under device processing conditions can control the functional yield of integrated circuits fabricated using electron-beam technology. This report describes several electrical and optical evaluations of oxide pinhole density related to process induced defects in PBS and TI-313 electron resist films. Such pinholes are believed to be the cause of the zero functional yield observed on first lots of 256-bit bipolar RAM circuits fabricated with PBS resist. Results of these comparative tests indicate that the TI-313 electron resist and associated processing gives significantly better film continuity and step coverage than the PBS, being comparable to commercially available photoresist. It is thus concluded that implementation of the TI-313 electron resist technology into the process sequence already established will permit fabrication of working 256-bit bipolar RAM circuits in the immediate future.

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IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Fifth Quarterly Report

1 September 1977 – 1 December 1977

Dr. G. L. Varnell
Mr. R. A. Williamson
Mr. G. A. Brown
Dr. T. L. Brewer
Dr. J. L. Bartelt
Dr. R. A. Robbins
Mr. C. D. Winborn

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FABRICATION OF 256-BIT BIPOLAR RAM

A. TEST RESULTS

Lot 3 of the e-beam 256-bit bipolar RAMs has been completed and all slices of the lot have been evaluated. One slice was processed through scribe and break, and enough chips from that slice were assembled to ship 50 engineering samples. The slices were evaluated using three different techniques. A description of each technique and the corresponding results are discussed below.

1. Visible Examination Using Optical Microscope

After the slices had been processed through the sinter step they were examined under an optical microscope using magnifications between 50X and 400X. In general, the edge quality and size control of all the geometries were quite good. There was, however, a substantial number of defects, normally referred to as pinholes, in the oxide patterns. Based on other data in this report, it is believed these pinholes were caused by PBS, the positive electron resist used at all the oxide removal steps. In our estimation, these pinholes were the predominant cause of the function failures.

2. Component Evaluation Using Three-Point Probe

After the visible examination was complete the individual components, such as resistors and transistors, were evaluated to determine their electrical characteristics. This procedure involved using a stage and three individual probes that were connected to a Tektronix 576 curve tracer. Each individual probe was placed on an aluminum pad which was connected to the appropriate node of the device. Then, using the appropriate function generators in the curve tracer, the component characteristics were measured. The results from this test are summarized as follows:

COMPONENT ELECTRICAL PARAMETERS
(NPN Output Transistor)

Parameter	Design Limits	Measured	Units
h_{FE}	20-100	48-64	
BV_{CEO}	5.0 V min	6.8-9.5	volts
BV_{CBO}		18-24	volts
BV_{EBO}		5.6-5.8	volts

Diffused Resistor

Parameter	Design Limits	Measured	Units
BV resistor to epi	7.0 V min	18-24	volts
Resistance	4.5-6.7	5.6-6.3	ohms

It is obvious from examining the data that the measured parameters are well within the design limits for the device. This data indicates that the diffusion processes that have been developed for fabricating the device are quite acceptable. Any chip having components with these characteristics should not fail because of electrical problems.

3. Circuit Evaluation Using HSM

After the three-point probe analysis, the slices were electrically tested using the High Speed Machine (HSM). This machine performs all the dc tests required to meet the contract specification. A summary of the measured parameters, test conditions and test limits is presented.

Parameter	Test Conditions	Limits Min	Limits Max	Measured	Units
Low-Level Output Voltage V_{OL}	V_{CC} = 4.5 V, I_{OL} = 10 mA		0.45	0.476*	volts
Input Low Current I_{IL}	V_{CC} = 5.5 V, V_{in} = 0.45 V	−5	−510	−35	μA
Input High Current I_{IH1}	V_{CC} = 5.5 V, V_{in} = 2.4 V		25	0.3	μA
Input High Current I_{IH2}	V_{CC} = 5.5 V, V_{in} = 5.5 V		1	0.003	mA
Output Leakage Current I_{CEX}	V_{CC} = 5.5 V, V_{out} = 5.5 V		100	0.8	μA
Input Clamp	V_{CC} = 4.5 V, I_{in} = −10 mA				
Diode Voltage V_{IC}	T_A = 25°C		−1.5	−0.75	volts
Power Supply Current I_{CC}	V_{CC} = 5.5 V, All inputs open		145	45	mA

*When the packaged units were tested, this parameter measured 0.389 V.

All the electrical parameters except V_{OL} were well within the contract specifications. Since V_{OL} was the only failing parameter, the slices were tested again with the V_{OL} test eliminated. The results were the same. It appears this parameter measured high because of the probe contact resistance since after the units were packaged and re-tested, this parameter measured only 0.389 V.

Two other basic tests were performed along with the above electrical tests. They were the continuity and function tests. The continuity test is performed by putting a bias on the device pins and biasing them using a low voltage (<1.5 V) to see if current will flow into or out the device pins. If current flows, the device passes the test. This test mainly checks to see if the contact windows were free of oxide and if the aluminum alloyed into the contacts. The functional test is a gross test to see if the circuit operates as a memory. During these tests, information is attempted to be written into and read from the memory. The device must meet only minimal electrical requirements to pass this test. The main purpose of the test is to see that the device "functions" as it should. This test gives a measure of the degree of pattern integrity on the device. If there are large numbers of pattern defects, they will manifest themselves as functional failures. Approximately 85% of the units passed the continuity test but 0% of the units passed the functional test. The 100% functional failures in conjunction with the results from the visible examination led to the conclusion that pinholes were the primary cause of device failures. This problem has been extensively discussed. It is believed that as soon as the TI-313 resist is phased in, the next lots of material will have some good memory circuits.

SECTION II
ELECTRON RESISTS

A. INTRODUCTION

This section describes a series of tests performed to evaluate the continuity of various positive electron resists under device processing conditions. They are important because their results demonstrate that PBS resist used as was done in the earlier parts of this program can produce pinholes during oxide removal operations at a level sufficient to cause the circuit functionality problems which have delayed contract completion. Of greater importance is the fact that the most recent tests show that TI-313 electron resist evaluated under the same conditions yields greatly reduced defect densities, being comparable to those found with commercially available photoresist films. On this basis it can be concluded that implementation of the TI-313 technology should permit fabrication of the required memory circuits in the immediate future.

One of the initial program plans was to use positive electron resists for all of the oxide removal steps. This decision was made because it reduced the relative area of the chip that would have to be exposed from 4/5 when using a negative resist to about 1/5 for positive resist. And, of course, slice exposure time is directly proportional to the amount of exposed chip area.

When the program commenced, there were only two positive electron resists available for use, PMMA and PBS. Since PMMA was too slow to meet the contract requirements, PBS was chosen. PBS had given good results in fabricating several test bars. However, when the first integrated circuit wafers were evaluated, it was realized that there were a significant number of visible defects in the oxide areas of the chips. It is believed this high defect density was the cause of the functional failures on the devices tested.

At the same time, similar problems were being found on some devices built on TI internal programs. However, these devices had fewer levels patterned using PBS so the cause of the defect problem was not clear. These problems precipitated the defect density studies of PBS. Two different approaches were taken to evaluate the resist. The first was a technique to measure the number of defects visually. The other was an electrical measurement of the defect density. The procedures and results of both techniques are presented later in this report.

B. VISIBLE EVALUATION TECHNIQUE

1. Slice Preparation and Evaluation Procedure

Unoxidized polished substrates were used as the starting material for the tests. They were then processed through a number of steps until ready for evaluation. Two separate runs of slices were made at different times using different bottles of resist. However, both bottles had essentially the same characteristics.

The first run involved only PBS and control slices. The second run included PBS, a negative photoresist, Kodak 747 and control slices. The procedure used to prepare the slices for the first evaluation consisted of the following steps:

1) Clean polished substrates
2) Oxidize at 1000°C to 9000 Å
3) Steam slices @ 700°C
4) Coat slices with PBS
5) Bake slices
*6) Develop slices
*7) Bake slices
8) Etch slices in buffered HF until back sides clear
9) Strip resist
10) Etch slices in planar etch
11) Strip oxide

*Used on 1/3 of the slices

The control slices went through steps 1, 2, 10 and 11 only. The thickness of the PBS after step 5 was approximately 4000 Å.

The technique used to prepare the slices for the second evaluation consisted of the following steps:

1) Clean polished substrates
2) Oxidize @ 1000°C to 9000 Å
3) Steam slices @ 700°C

4) Coat slices with PBS or 747

5) Bake slices

6) Etch slices in buffered HF until back sides clear

7) Strip resist

8) Etch slices in planar etch

9) Strip oxide

One-third of the slices were coated with PBS, one-third were coated with 747 and one-third were used as control slices. The thickness of both resist films was 4000 Å. The control slices went through steps 1, 2, 8 and 9 only.

After the slice preparation was complete, the slices were examined for defects using an optical microscope. The planar etch enlarged the defects to approximately 1.0 to 1.5 mils in diameter which made them easy to see and count under the microscope.

2. Results

The results from the two runs are shown as follows:

RUN 1
Defects/cm^2

PBS	PBS w/steps 6 and 7	Control
0.94-2.46	1.16-3.84	0

RUN 2

PBS	Kodak 747	Control
34.6-46.6	1.40-5.29	0

The results from Run 1 indicate that the defect density increases by about 50% when the slices are run through the develop cycle, which of course is part of the normal resist process. There are 15.98 chips/cm^2 on the slice. Taking the worst case of 3.84 defects/cm^2/level, there would be on the average 19.2 defects/cm^2 after all oxide masking steps or a little greater than 1.2 defect/chip. Taking the best case of 1.16 defects/cm^2/level, there would be on the average 5.8 defects/cm^2 after all oxide masking steps or about 1 defect for every 2.76 chips. Under these circumstances there should have been some good devices in the lots.

The results from Run 2 are very discouraging. Using the best case of 34.6 defects/cm^2/level, there would be on the average about 173 defects/cm^2 after all oxide masking steps, or about 10.8 defects/chip. It would be practically impossible to get any good devices with a defect density this high. There is obviously some problem with the PBS since the defect density of the 747 was not nearly as high.

The reason for the variation in the defect density from one test to the next or for the very high densities found in Run 2 has not yet been determined. Further studies of the resist are continuing.

3. Adhesion Problems

PBS does not adhere very well to oxide surfaces, especially phosphorus glass oxides, necessitating a pretreatment of the oxide before applying the PBS. Normally slices see a nitrogen ambient just prior to being removed from the furnace tube. However unless the PBS is immediately applied upon their removal from the furnace, severe undercutting will result at that O.R. step. Immediate application of PBS is usually not feasible because of logistics problems so two alternative routes have been followed.

The routine procedure is to give the slices a low temperature (≈700°C) treatment in a steam ambient for 5 minutes prior to applying the PBS. This procedure works quite well but also has several problems. One is that it is an extra process step which increases cycle time and slice processing cost. Second, it cannot be used prior to contact O.R. because of its effects on transistor h_{FE}s at low temperatures and low I_Cs.

The other alternative procedure is to apply a silane film to the slices prior to the application of PBS. This procedure is done as follows:

1) Bake – IR @ 160°C
2) Coat – 2% Phenyltrichlorosilane (PTCS)/Xylene @ 5K RPM
3) Bake – IR @ 160°C
4) Coat – PBS

This procedure works well and was used at contact O.R.

Included are some photographs taken from blank oxidized slices that were patterned with PBS. Figure 1 was taken from a slice that had no treatment prior to applying PBS. Figure 2 shows a slice which had the steam treatment prior to applying PBS. Figure 3 was taken from a slice which had the PTCS treatment prior to applying PBS. These pictures are representative of the results achieved using these processes.

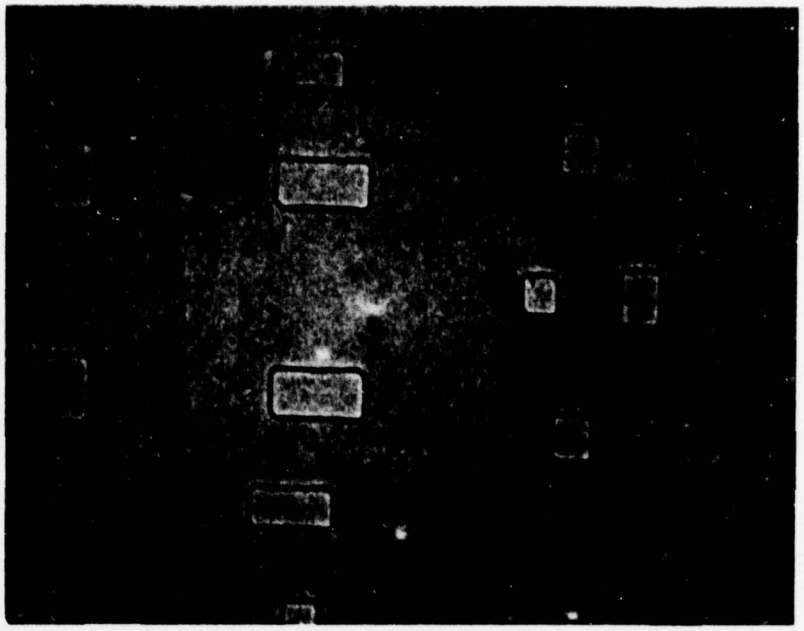


Figure 1. PBS Adhesion: No Pretreatment

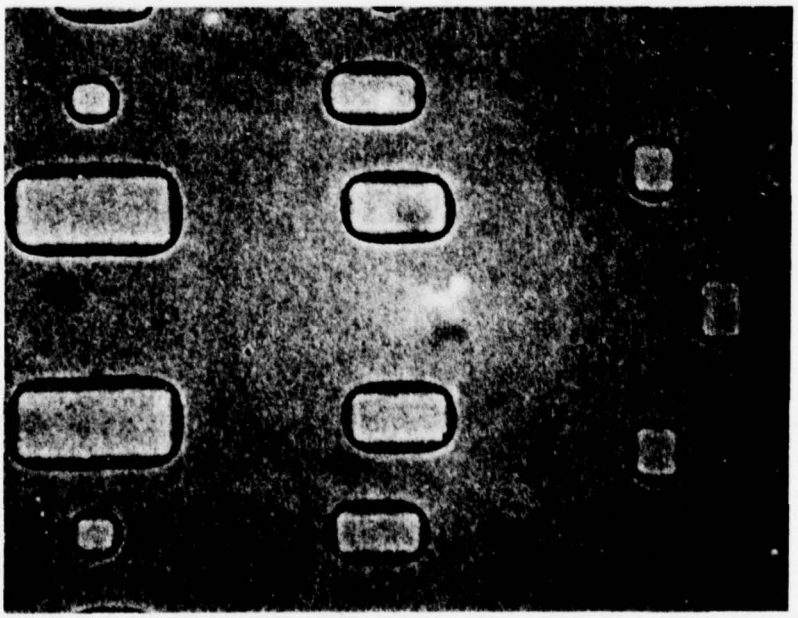


Figure 2. PBS Adhesion: Steam Pretreatment

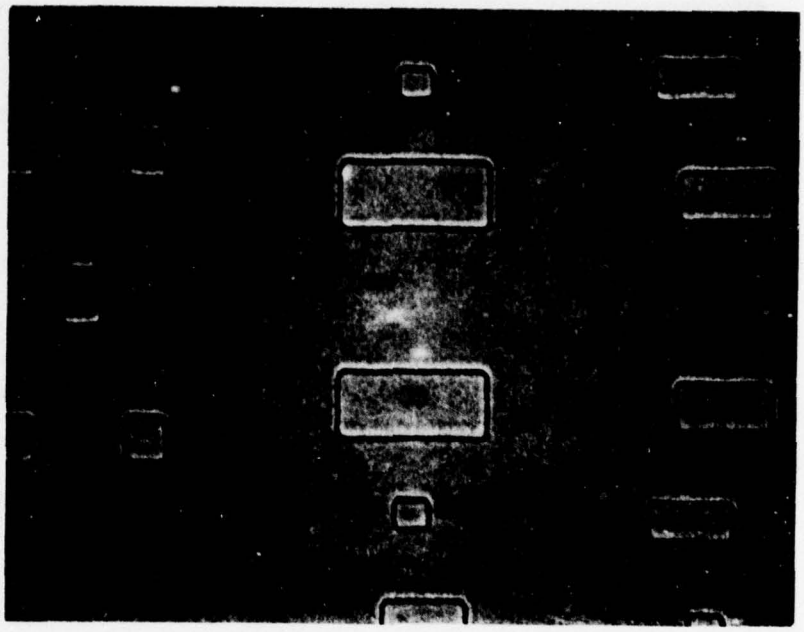


Figure 3. PBS Adhesion: Phenyl Trichlorosilane Pretreatment

C. ELECTRICAL EVALUATION OF RESIST CONTINUITY

1. Test Procedures

Device problems related to electrode-to-substrate short circuits and electrode discontinuity over thick-to-thin oxide steps suggest that PBS, as processed in these instances, was subject to localized attack and breakdown during development and etching. This was particularly true in the vicinity of surface irregularities but was also found in flat, unpatterned regions of the devices. A simple, quickly performed test was required to provide quantitative characterization of the magnitude of these two effects, and to serve as a vehicle for process improvement.

To meet this need, it was decided to fabricate large-area MOS capacitors on silicon dioxide films that had been entirely protected by electron resist during an oxide etching procedure that would 100% over-etch the film. Control wafers for oxide quality and processing were included in the tests. After etching and resist removal, aluminum was evaporated on the oxide, circular capacitors of various areas up to 0.02 cm^2 were formed, and the structures were sintered at 450°C for 50 minutes. If a void was present or had been formed in the resist during processing, the over-etching would form a pinhole in the oxide film, causing an MOS capacitor formed in that region to be shorted to the substrate during sintering. The incidence of such shorts was determined

by electrical breakdown measurements on arrays of these capacitors, normally 100 capacitors per wafer. Slice mapping techniques were used to locate the defects physically, and defect density was calculated on the basis of a Boltzmann statistical model.

a. SAMPLE FABRICATION

To simplify processing and measurement, thin oxides, nominally 850 Å thick, were used for these tests. Separation of the effects of attack in planar regions and at oxide steps was approached in two ways. The simplest and most rapid technique was to eliminate the effects of the steps by building capacitors on wafers oxidized in one step to a single thickness. Such tests provide a quick characterization of the level of attack, and can be compared to results on more complex wafers where thick oxides are initially grown, holes etched and reoxidized to 850 Å, and aluminum electrodes are aligned over the resulting oxide step.

A better procedure which evolved during the test program permitted exact simulation of the oxide steps occurring on the circuit arrays and direct comparison of flat surface and oxide step defects on the same slice. Such structures are shown in Figure 4, a photomicrograph of a test structure array containing a variety of circular and annular MOS capacitors. The small triangles are markers for alignment of the photomask levels. Considering only the two largest circular units in the array, circular areas of 0.01 and 0.02 cm^2 were protected by silicon nitride dots. Normal field oxides of one-micrometer thickness were grown surrounding these dots, after which the nitride was selectively etched away with 180°C phosphoric acid. Thin oxides (850 Å) were then grown in the regions where the nitride had been removed. After aluminum evaporation, a contact mask was aligned so that a 0.01 cm^2 dot was formed in the center of the 0.02 cm^2 thin oxide region (nested capacitor), and a 0.02 cm^2 electrode was formed overlapping the 0.01 cm^2 thin oxide region (overlap capacitor). The wafers were then sintered. This provides two interlocking arrays of capacitors of equal effective area (0.01 cm^2), one of which includes an oxide step at its outer perimeter (overlap) and one of which does not (nested). Having both arrays on a single wafer permits direct comparison of the effect of inclusion of the oxide step without concern for wafer-to-wafer variation due to processing variability.

With this general fabrication procedure, a variety of tests can be run in which wafers are coated after thin oxidation with electron resist or photoresist, developed, etched, and stripped, or any combination of these procedures in order to isolate the effects of the various processes.

The experiments described in this report were performed employing all of these fabrication techniques: single thickness oxides, nested and overlap capacitors on different wafers, and nested and overlap capacitors on the same wafer.

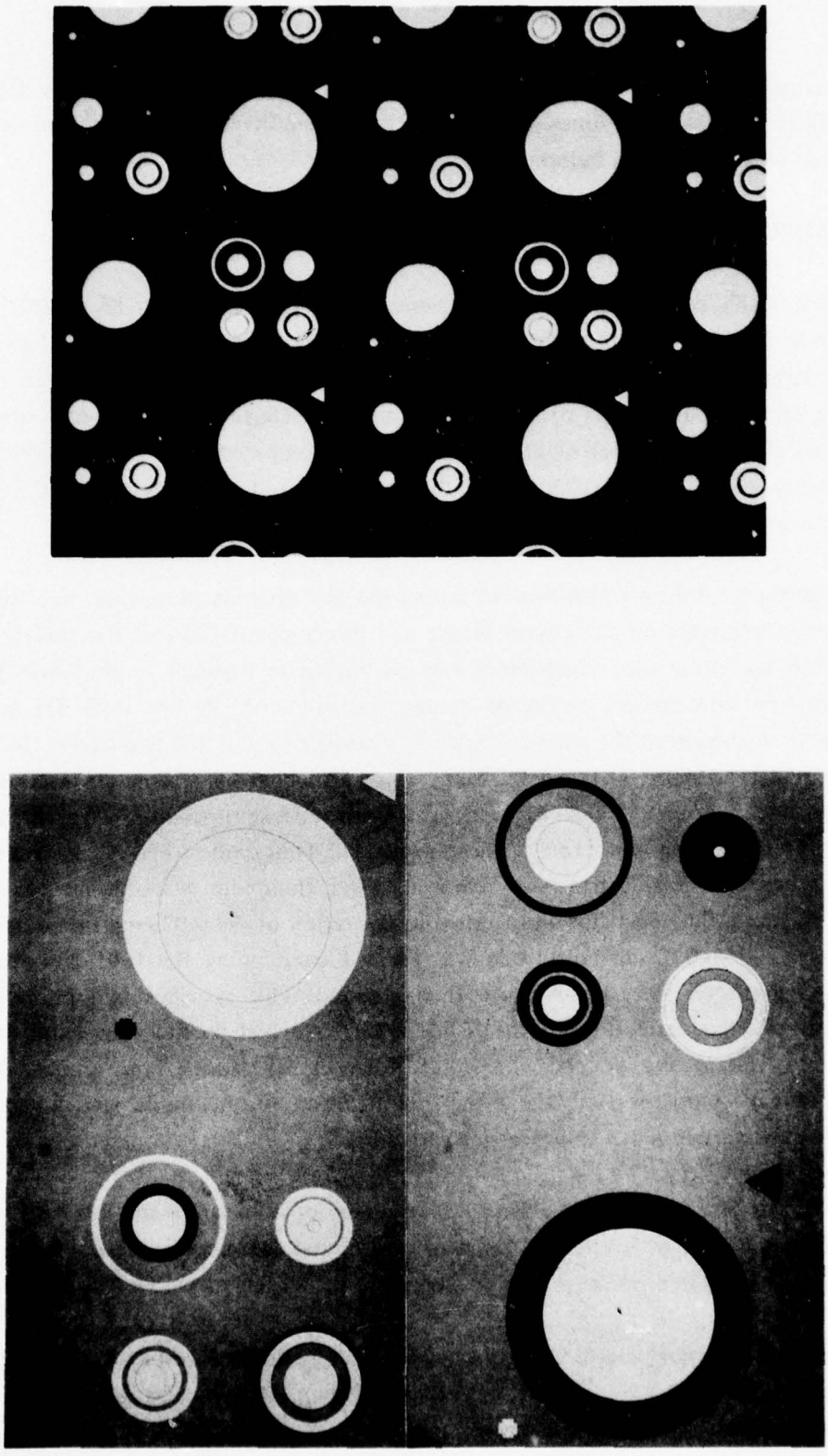


Figure 4. Array of Nested and Overlap MOS Capacitor Test Structures

b. ELECTRICAL CHARACTERIZATION

Because of the sample fabrication process, a void or pinhole in the resist film under test should result in a capacitor electrically shorted to the substrate silicon. These can be found by probing the capacitor array with a single low voltage, testing for any level of conductivity. However, other more subtle forms of damage may occur, due to slow attack and partial failure of the resist film, or damage to the underlying oxide by processes other than the etching, such as resist removal. Identification of these effects requires a more complex testing procedure, like that used for measurement of dielectric strength of insulating films. Three different test programs were used for these experiments, two of which were developed especially for this work. Two of them employ a sequence of voltage steps applied to the capacitor until a certain fixed level of conductivity is observed, while in the third, a voltage ramp of variable rate and amplitude is used. Automated data analysis was improved from a simple compilation of breakdown voltage versus frequency to inclusion of slice mapping capability, probability plot generation, and automated defect density calculation.

The first testing was done using a standard integrated circuit tester. A staircase of −6-volt steps was applied to the test capacitor; 50 milliseconds after each step, the current flowing through the capacitor was measured. If the current was greater than 40 microamps, the capacitor was assumed to have been broken down by the last step and the final voltage was measured, recorded, and the prober was moved to the next capacitor. After the desired array had been broken down, a frequency distribution of breakdown voltages was tabulated, and the percent of the sample broken down at each voltage step was computed. Considerable manual data manipulation was required to extract information from this tester, but it was adequate for identification of gross short-circuit data.

The second test program was built around a Hewlett-Packard 9830 automated measurement system, and included many improvements both in measurement versatility and data analysis. A staircase of voltage steps was still used, but either positive or negative polarity could be generated, any step amplitude and number of steps could be selected up to a maximum voltage of 100 volts, and both step duration and current measurement delay after step application could be varied. Most common values used were one second and 200 milliseconds, respectively. In addition, any trigger current level above a fraction of a microamp could be selected. Arrays of any size up to 25 X 25 units could be probed automatically. Data analysis capability included a frequency distribution of breakdown voltages, a table of cumulative percent of the sample broken down up to and including each voltage level and a computation of defect density based upon the assumption, following Osburn and Ormond,[1] that any unit with a breakdown voltage less than 0.8 times the

1. C. M. Osburn and D. W. Ormond, *J. Electrochem. Soc.*, Vol. 119, No. 5, 591 (May 1972).

maximum breakdown voltage found in the sample is defective. Also useful in data interpretation is the slice mapping capability, which plots the capacitor array identifying any units with breakdown voltage below any chosen value. This mapping is iterative in nature, and any number of maps may be generated from each data set to identify the location of units found in the data tables. This is of value in identifying slice edge or array corner units which have a higher probability of being defective due to handling, and in determining proximity of defective units possibly caused by scratches on the wafer surface. Following the generation of slice maps, a graph of breakdown voltage versus cumulative percent of sample is plotted on a probability scale. This type of graph has the property that a Gaussian data distribution will plot as a straight line. If such a straight line is found when data is plotted, the standard deviation of the distribution can be obtained from the slope, and the extent of the sample which is not a part of the overall normal distribution can be determined. This break point in the curve provides perhaps the best estimate of defect density, wherein a defect is defined as any departure from the characteristics of an ideal statistical sample. Great care must be used in the interpretation of these results.

A ramp voltage supply system was substituted for the voltage staircase in the third measurement setup developed. The ramp, generated by the charging of a large fixed capacitance by a constant current source, has a rate variable upward from 10 volts/second. Rates as high as 120 volts/second have been used experimentally. One degree of freedom lost with this system is that the failure trigger current level is determined by the hardware to be 40 microamps. Rate experiments performed on interlocking arrays of capacitors on the same wafer indicate that breakdown characteristics are invariant for rates of 20 volts/second and greater. A barely discernible indication of time-dependent effects is noticeable when slowing the ramp to 10 volts/second.

It is difficult to compare results of the ramp and staircase test procedures in great detail because of these time-dependent effects. Minimum step duration of the staircase system is about one second, limited by hardware. This sets an upper practical limit on effective ramp rate at about 5 volts/second in order to maintain acceptable distribution definition of the sample. As mentioned, the voltage ramp system has a minimum rate hardware limited to 10 volts/second, making it impossible to test samples with both systems at the same effective ramp rate. However, ramp and staircase measurements done on interlocking arrays at 10 and 5 volts/second, respectively, were very similar in appearance. Median breakdown voltages were, in general, less than 10% higher with the staircase system. This difference might be expected, in that with the staircase system, a steady current at the failure level must be measureable twice, at 50-millisecond intervals, before a unit fails; whereas with the ramp system, the first current pulse above the failure level defines a failure. In this regard, both systems might be useful in that they tend to separate the effects of early self-healing breakdown from complete catastrophic failure. For these measurements, thick aluminum films (greater than one micrometer) were used to inhibit formation of self-healing defects.

Several different definitions of defect density are used in these experiments, and it is important to understand these definitions and the manner in which the computations are made. As mentioned above, the fabrication of these test samples was done in such a way as to cause electrically shorted capacitors to be formed if voids occurred or were etched in the resist films. For this defect mode, the occurrence of failures at the first step of the voltage staircase or at some arbitrarily low ramp voltage (usually taken as 10 volts) was monitored. Such data is usually reported here as the percent of failed units relative to the total number measured. For the case of 100 capacitors each of 0.01 cm^2 area, this percentage defective is very nearly equal to the defect density per square centimeter computed from the statistical models described below. With this in mind, data on electrically shorted units can be correlated with the visible defect densities measured in Section II.B of this report. Similarly, units which were capable of withstanding some voltage stress but which failed well below the voltage range at which most units failed were separated into a secondary defect category. Such defects may be related to partial resist failure or oxide or silicon surface damage caused by cleaning or resist removal processes.

Two slightly different defect densities are generated by the automated tester, both defined in terms of departures from idealized statistical behavior of a defect-free film. The first follows the experimental determination of Osburn and Ormond that breakdowns between the maximum observed breakdown voltage and 0.8 times that value may be associated with the intrinsic breakdown characteristics of the film. By this definition, any unit with a breakdown voltage below this lower limit has a defect associated with it. The extent of the primary or intrinsic breakdown distribution is thus given by unity minus the fraction of units tested having breakdowns less than 0.8 times the maximum breakdown voltage. This probability of finding primary mode breakdowns, Y, is converted to defect density using the Boltzmann model:

$$\ln (Y) = -A \times D \qquad (1)$$

where

D = defect density (cm^{-2})

A = sample area (cm^{-2}).

Arguments for the validity of the use of this expression have been presented by Chou and Eldridge.[2]

The second approach to the definition of a defect density relative to the intrinsic breakdown properties of the oxide makes use of the probability plot of breakdown voltage versus cumulative percent of sample generated by the automated system. After completing the plot, the operator

2. N. J. Chou and J. M. Eldridge, *J. Electrochem. Soc.*, Vol. 120, No. 8, 1139 (August 1973).

inspects it to determine the existence of a straight line indicating a Gaussian distribution of breakdown voltages in the primary voltage range. If such a distribution does exist, its extent is noted from the graph, and the yield of such primary units is entered into the system, which then computes a defect density using equation (1). In most cases, good agreement has been observed between these two techniques for defect density calculation, tending to confirm the observations of Osburn and Ormond.

Other workers[3] have argued that because of the nature and source of oxide defects that another expression:

$$Y = \frac{1}{1 + A \times D} \qquad (2)$$

is a more valid representation of the relationship between yield, sample area, and defect density. For values of $A \times D$ much less than unity, equations (1) and (2) are very nearly equal, and the percent difference is only 44% when $A \times D = 1$. Figure 5 is a plot of the two relationships for the case of $A = 0.01\ cm^2$, the most commonly used value in these experiments.

2. Test Results

Four tests will be described which employ the procedures described above to evaluate the continuity of both PBS and TI-313 electron resists under device processing conditions. The first two experiments using PBS, examine attack on single thickness oxide films and the effect of resist thickness on oxide step coverage.

a. EXPERIMENT G: SINGLE THICKNESS OXIDES/PBS

The aim of this experiment was to determine the pinhole density in an oxide film resulting from the use of PBS electron resist for an oxide removal process on single thickness, unstepped oxides. Twelve wafers were used, divided into three cells of four each. The first cell was a control on the quality of the oxide as grown. No resist coating or etching was performed on these wafers. The purpose of the second cell was to separate the effects of resist application, processing and removal from those associated with attack during etching. Wafers in the third cell were subjected to complete resist and 100% over-etching processes while completely coated with resist.

All wafers were cleaned by standard preoxidation techniques and oxidized to a 600 Å thickness in dry oxygen at 1100°C. Cell nos. 2 and 3 wafers were then coated with PBS and baked as usual for an oxide removal process. Cell no. 3 wafers only were then etched in common oxide

3. R. L. Meek and R. H. Braun, *J. Electrochem. Soc.*, Vol. 119, No. 11, 1538 (November 1972).

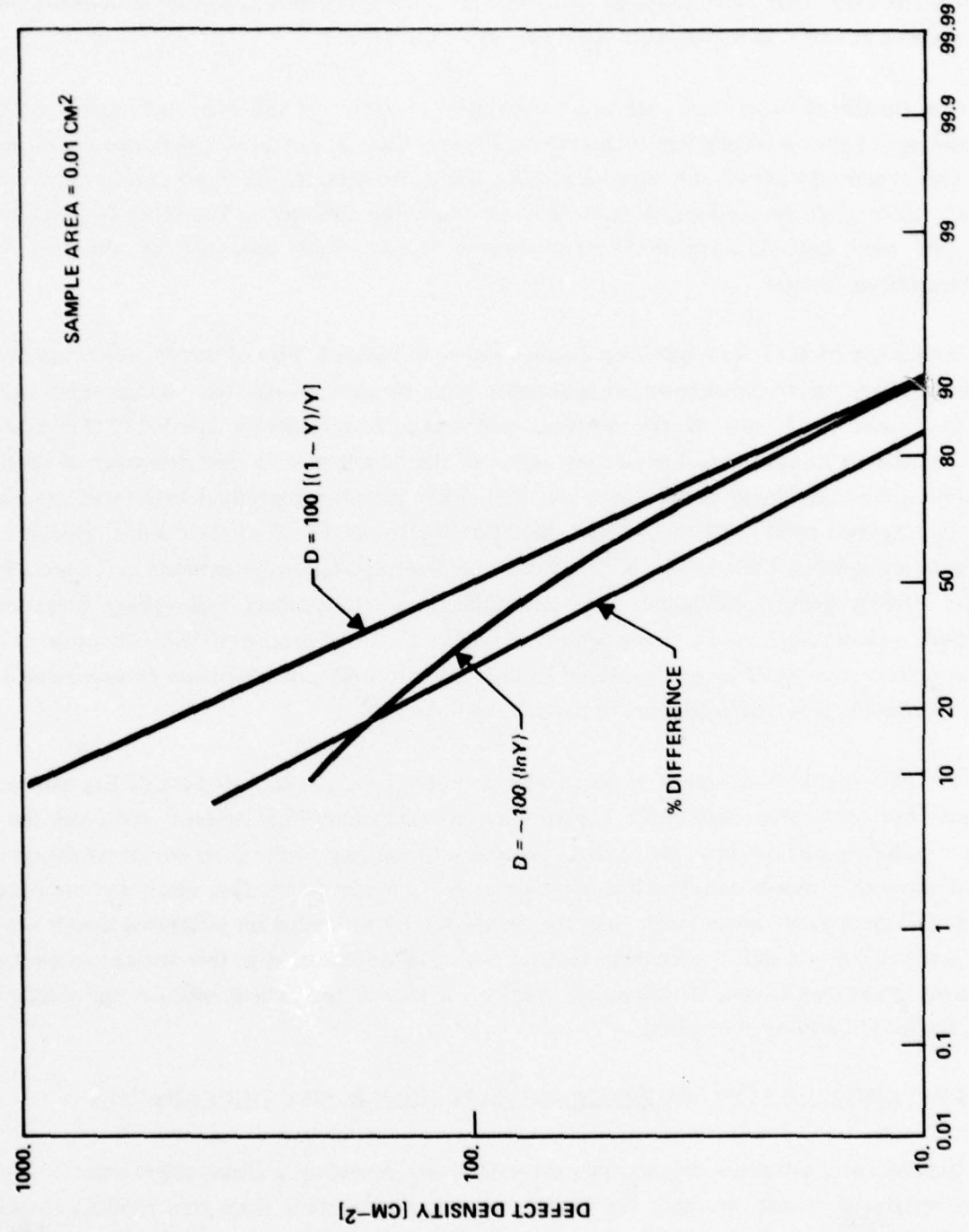


Figure 5. Comparison of the Yield-Defect Density Relationship for Two Statistical Models

etch for a time sufficient to remove twice the oxide thickness present, or 1200 Å. After resist removal on wafers in cells 2 and 3, three wafers from each cell were then coated with pure aluminum evaporated for an induction heated source, the aluminum was patterned on two of the three wafers from each group using the circular array shown in Figure 1, and all aluminized slices were sintered at 450°C in a 50-minute N_2-H_2-N_2 cycled ambient.

One metallized wafer from each cell was stripped of aluminum and examined microscopically for evidence of silicon pitting due to aluminum alloying through pinholes. The unmetallized slices were also examined optically for signs of etching attack. No clearcut differences in the appearance of these slices could be resolved, dependent upon processing differences. The other two wafers in each cell were probed using the first integrated circuit tester described in the Electrical Characterization section.

Probability plots of the breakdown data are shown in Figure 6. Five of the six wafers have very similar primary mode breakdown distributions, with median breakdown voltages just below 50 volts. Wafer no. 7, one of the resist-no etch group, had markedly inferior characteristics, probably due to mishandling. The striking aspect of the data is seen in the percentage of shorted units, those breaking down at the first 6-volt step. While the four nonetched wafers had losses less than 2%, the two resist-protected, etched slices lost 10.1% and 12.9% of their units, respectively. This data is shown in Table I. This is strong evidence for resist failure as outlined in the preceding section. Defect density computed from deviations from the primary high-voltage breakdown distribution shows only a weak dependence on resist and etching processes. This is because of the relatively large number of secondary mode breakdowns probably resulting from damage related to silicon surface preparation, oxidation, or handling processes.

The relatively high incidence of shorted units observed on the etched slices of Experiment G supports the contention that under normal process conditions, PBS electron resist can fail to protect underlying oxides in oxide removal processes. Conversion of the short circuit results on the etched slices to a defect density gives approximately 12 defects/cm^2. This value, and even those shown on Figure 6, are much lower than the defect density estimated on integrated circuit wafers from test bar data. In order to confirm that the resist failure observed in this test can account for the gross integrated circuit functionality problem, a second test which includes the effects of nonplanar oxide surfaces is required.

b. EXPERIMENT J: STEP COVERAGE AND ELECTRON RESIST THICKNESS/PBS

Experiment J advances the previous experiment by providing a closer approximation to an actual integrated circuit structure for pinhole testing. Oxide steps from thin (850 Å) to thick (10,000 Å) layers were formed using the recessed oxide approach described in the Test Procedures

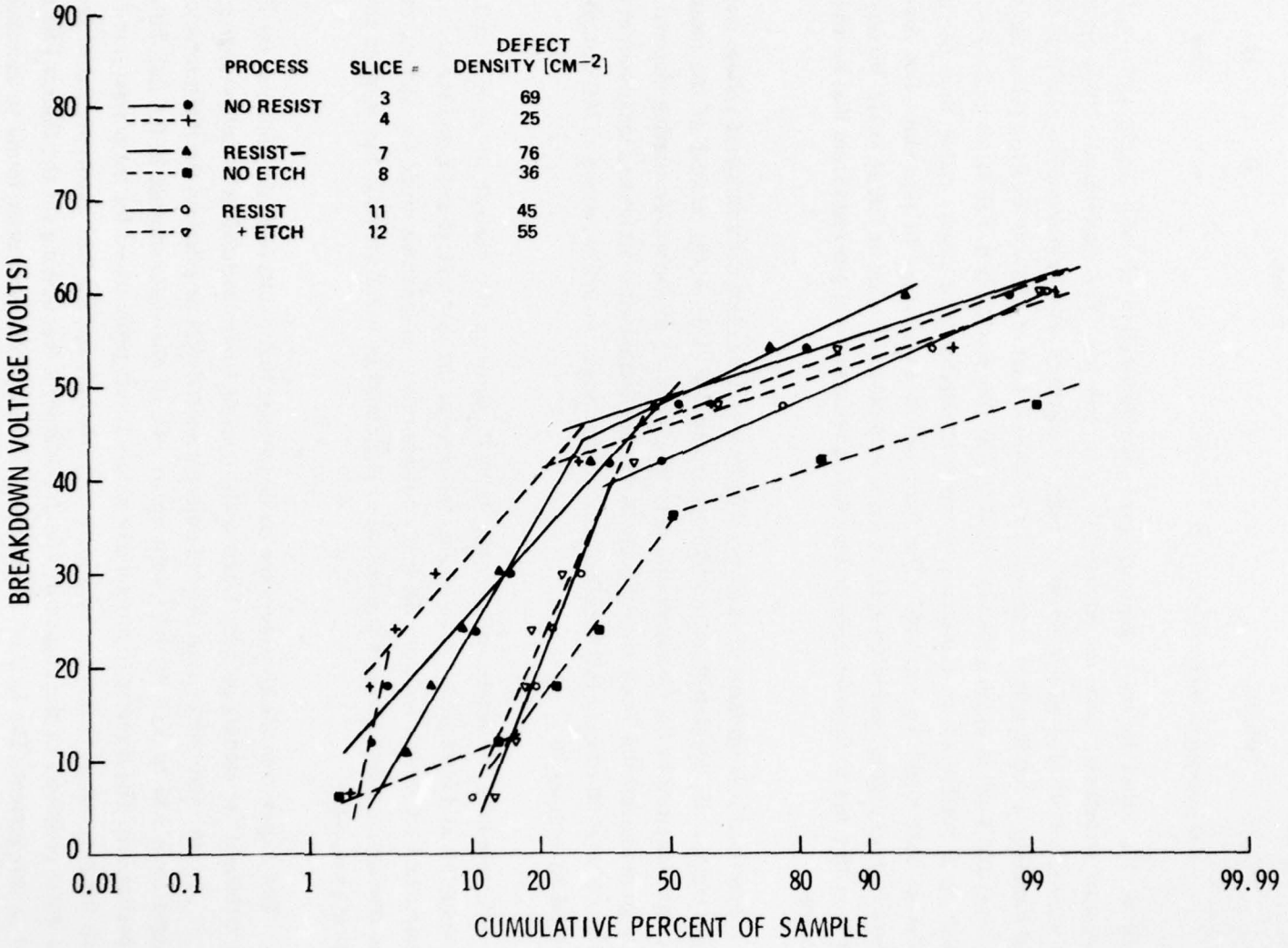


Figure 6. Experiment G: Thin Oxide Integrity Associated with E-Beam Resist Pinholing

Table I. Experiment G: Single Thickness Oxides/PBS – Shorted Capacitor Data

	No Resist		Resist No Etch		Resist + Etch	
Slice No.	3	4	7	8	11	12
% of units with BV less than 6 volts	0	1.97	1.79	0	10.1	12.9

section. Variations in mask sequence permitted fabrication of both nested and overlap MOS capacitor structures, done on separate slices in this test. The experiment, which encompassed 27 wafers, was divided into three major cells: a control on surface preparation, cleaning, oxidation, and handling; a cell in which a normal 4000-5000 Å coat of PBS was used to protect against oxide etching; and a cell in which a thicker (9000 Å) PBS film was applied. This latter technique had been tried on a portion of an integrated circuit lot, yielding poor results rather than the improved coverage that might be expected. The third cell is an attempt to reproduce this result under controlled conditions, and if possible, to relate it to the oxide pinhole failure mode. No attempt was made in this test to separate damage done during resist removal processes from that incurred during etching.

Electrical measurement of oxide breakdown was done using the automated voltage step system built around the Hewlett-Packard 9830 minicomputer. This is the second of the measurement systems described in the Characterization section. Because of the n-type starting material, positive voltage in incremental 2-volt steps was applied at one-second intervals up to a maximum of 90 volts, at which level all of the capacitors had been broken down. As before, arrays of 100 capacitors were probed on each wafer.

A summary of results is given in Table II, showing the percent of units found shorted (conductive at a level greater than 10 microamperes at the first voltage step), and the defect density computed from deviations from the high-voltage primary breakdown mode for each of the nested and overlap capacitor slices. A comparatively high level of wafer breakage has reduced the sample size in some cells.

This experiment clearly shows the oxide damage that results from the failure of the PBS films to withstand the etching process. Whereas the control groups had defect densities ranging from 23 to 52 per cm^2 and one or zero shorted units per slice, defect densities on the PBS-protected wafers ranged from 146 to 321 per cm^2 with up to 74% of the units shorted in the thin PBS overlap capacitor cell. The inability to protect oxide steps is very pronounced for the normal thin PBS films with the percentage of shorted units increasing from 2% to 50% with incorporation of the step at the outer periphery of the capacitor. The degradation is less striking for the thicker PBS material, but is still present. The lack of improvement in circuit characteristics found in increasing resist

Table II. Experiment J: Gate Oxide Integrity After First Oxide Removal

Sample	Slice No.	Defect Density (cm^{-2})	Shorted Units (%)
Control – Nested	1	37	0
	3	35	0
Control – Overlap	4	52	1
	5	23	0
	6	46	1
Thin PBS – Nested	10	146	2
Thin PBS – Overlap	13	230	74
	14	204	61
	15	240	15
Thick PBS – Nested	20	321	4
	21	281	2
Thick PBS – Overlap	24	240	6

thickness mentioned above is borne out in the defect density data, which for both nested and overlap structures, shows equal or reduced oxide quality. The magnitude of the defect densities seen here is comparable to those suggested by IC plug bar data, which had not been true in previous simpler tests.

Many of these degradation effects can be most clearly judged by examining the breakdown distributions themselves, so probability plots of breakdown voltage versus percent of sample are shown in Figures 7 through 12 for one wafer from each of the six groups. As can be seen from Table II, wafer-to-wafer uniformity within a subgroup was good. An example of the value of the breakdown distribution plots in data interpretation is seen by overlaying Figures 11 and 12, the thin and thick PBS-overlap capacitor structure data from slices 13 and 24. The percentage of defective units in the two distributions is seen to be very nearly equal, but in the case of the thin PBS film, most of the units were shorted, indicating complete resist failure, while the thicker PBS resist failure was only partial or delayed, yielding capacitors that would break down below 20 volts. The overall poor quality of these results dictates a search for an improved resist material, or at least improved processing techniques for PBS.

c. EXPERIMENT N: SINGLE THICKNESS OXIDES/TI-313

As a result of the poor yield results obtained with electron-beam processing of complex integrated circuits using PBS, accelerated effort was directed toward development and implementation of TI-313 electron resist. As soon as basic processes were established, this preliminary test of resist continuity under oxide etching conditions was performed. Single thickness oxides grown to 850 Å in dry ambient at 1100°C were used for the test.

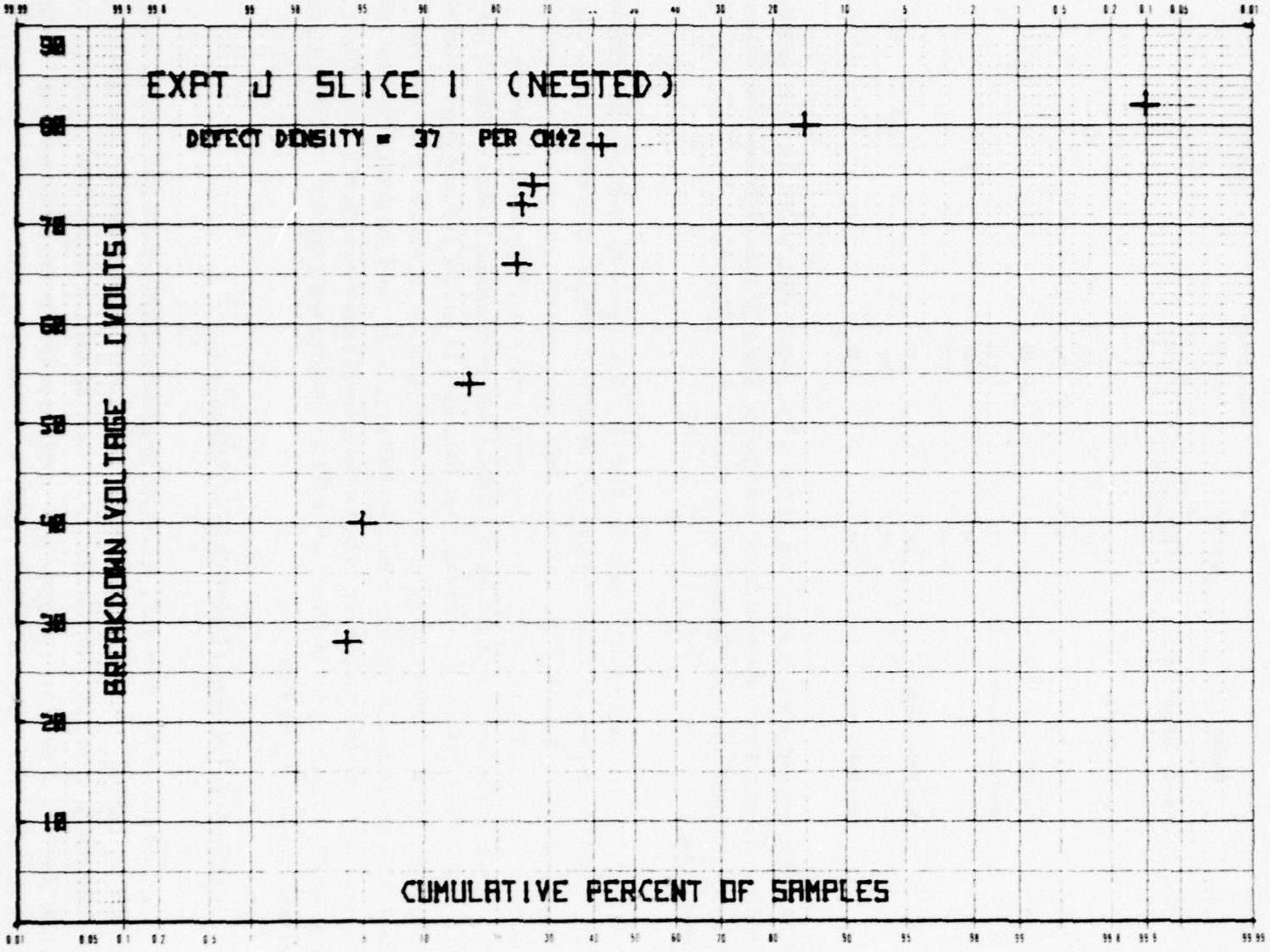


Figure 7. Experiment J: BV Distribution for Nested Control Samples

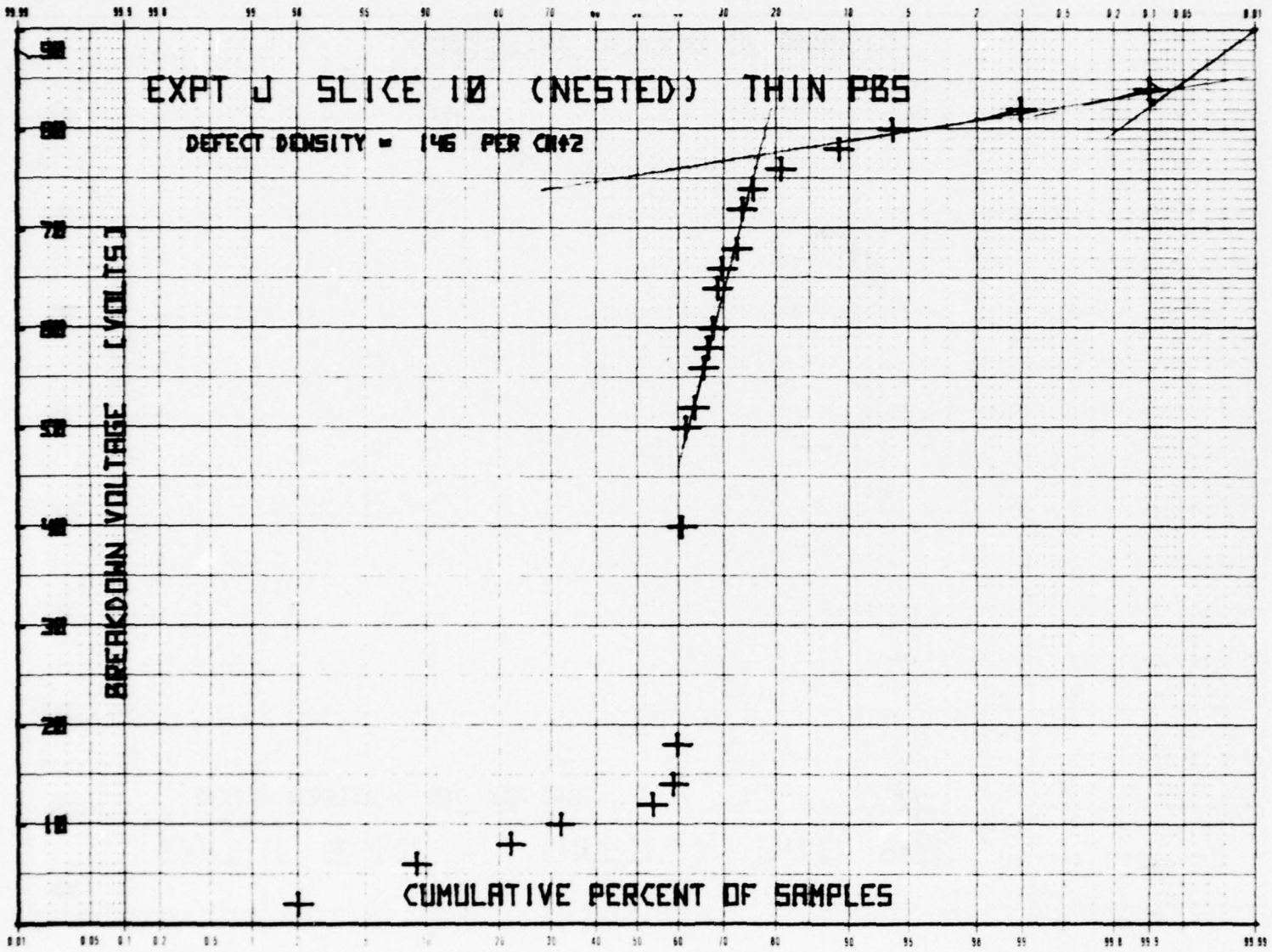


Figure 8. Experiment J: BV Distribution for Nested Samples Protected with Thin PBS

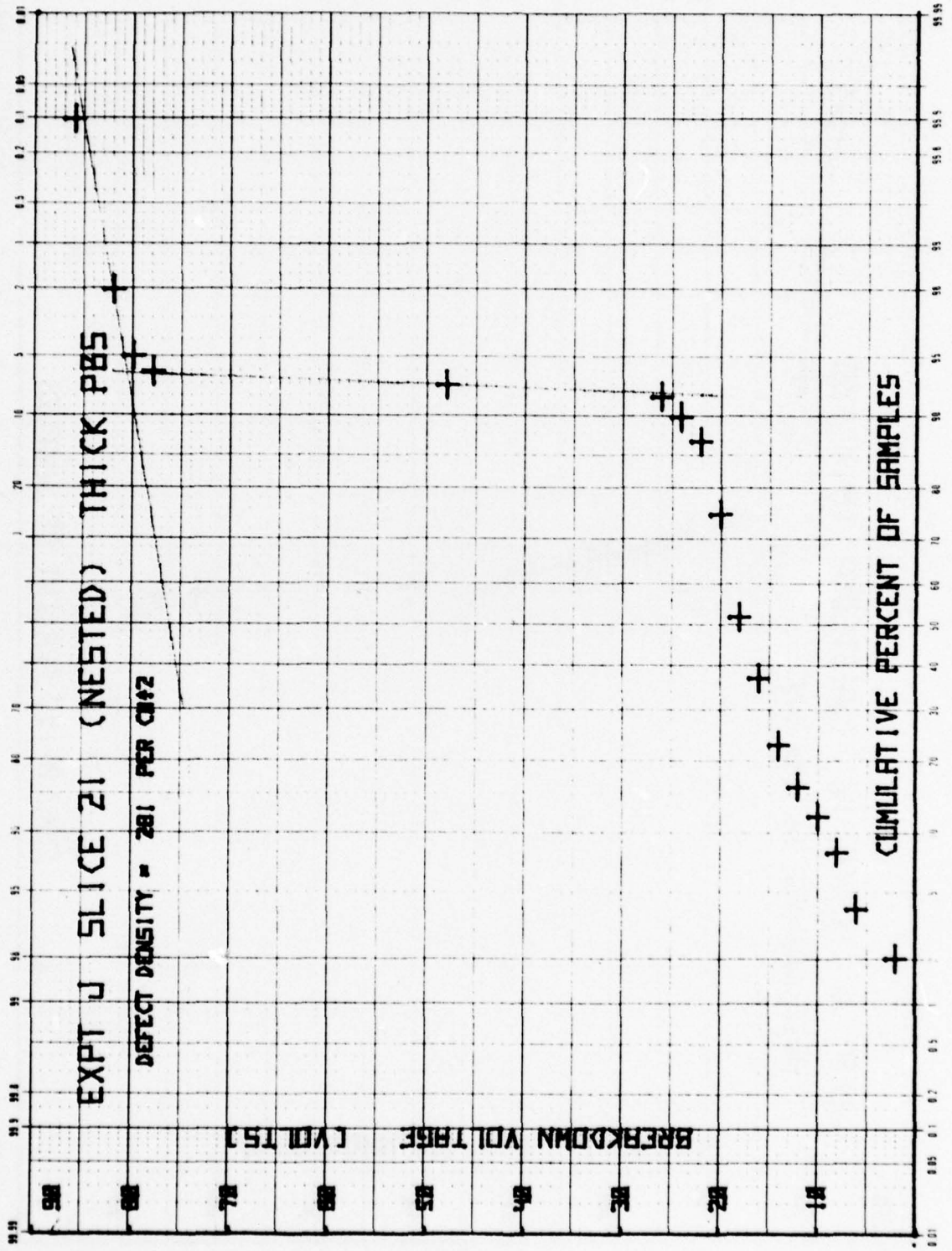


Figure 9. Experiment J: BV Distribution for Nested Samples Protected with Thick PBS

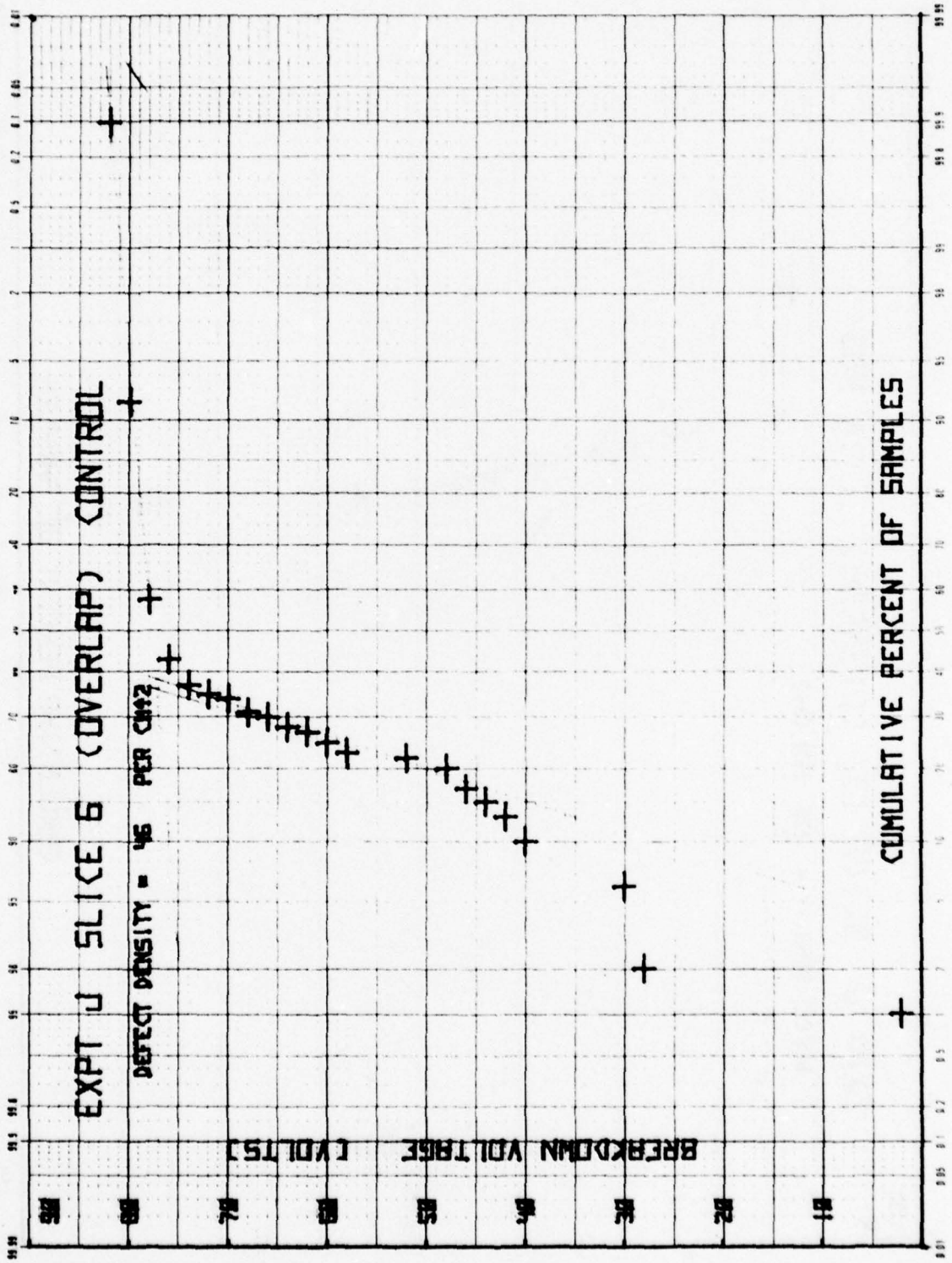


Figure 10. Experiment J: BV Distribution for Overlap Structures (Control)

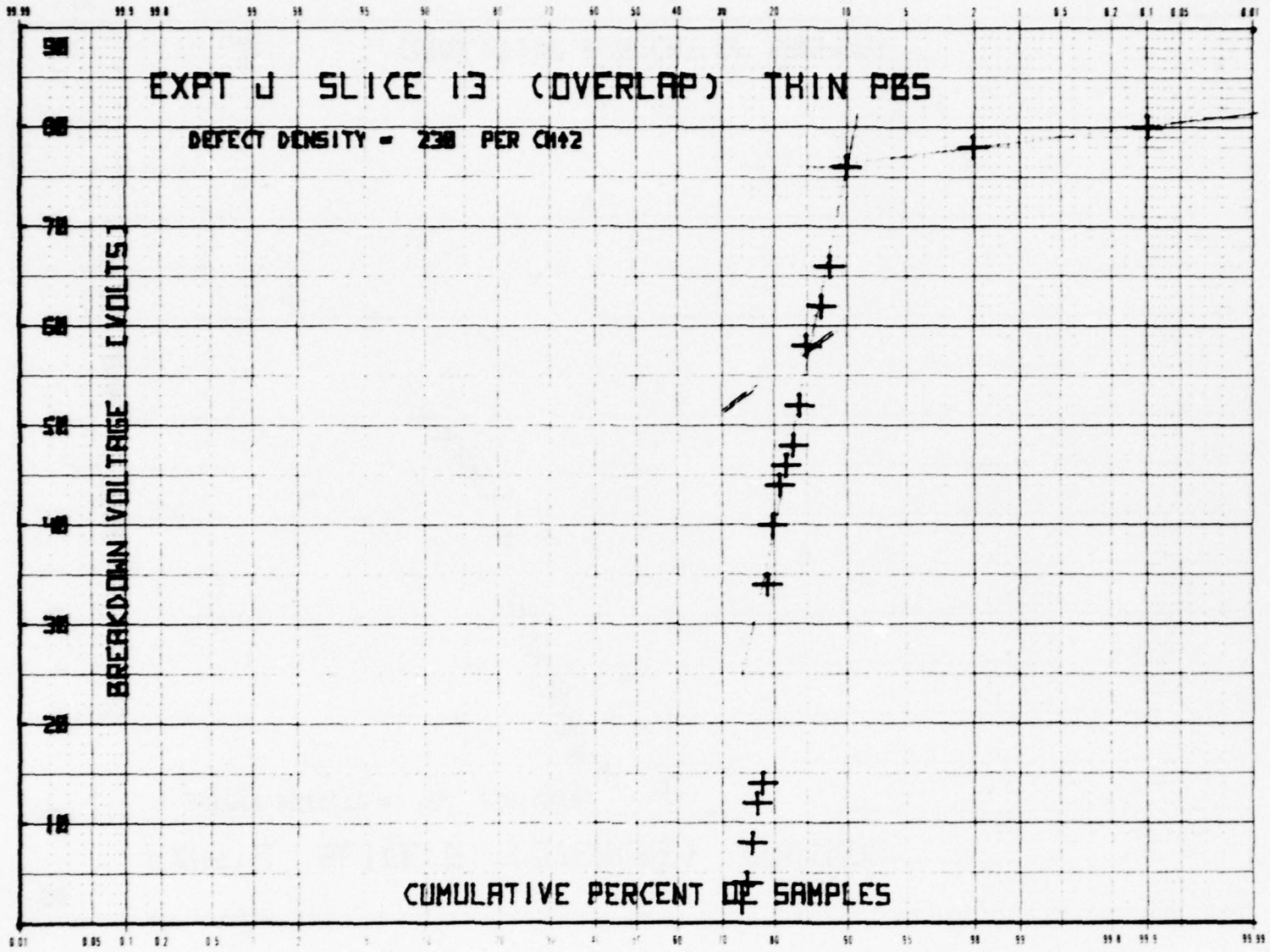


Figure 11. Experiment J: BV Distribution for Overlap Structures Protected with Thin PBS

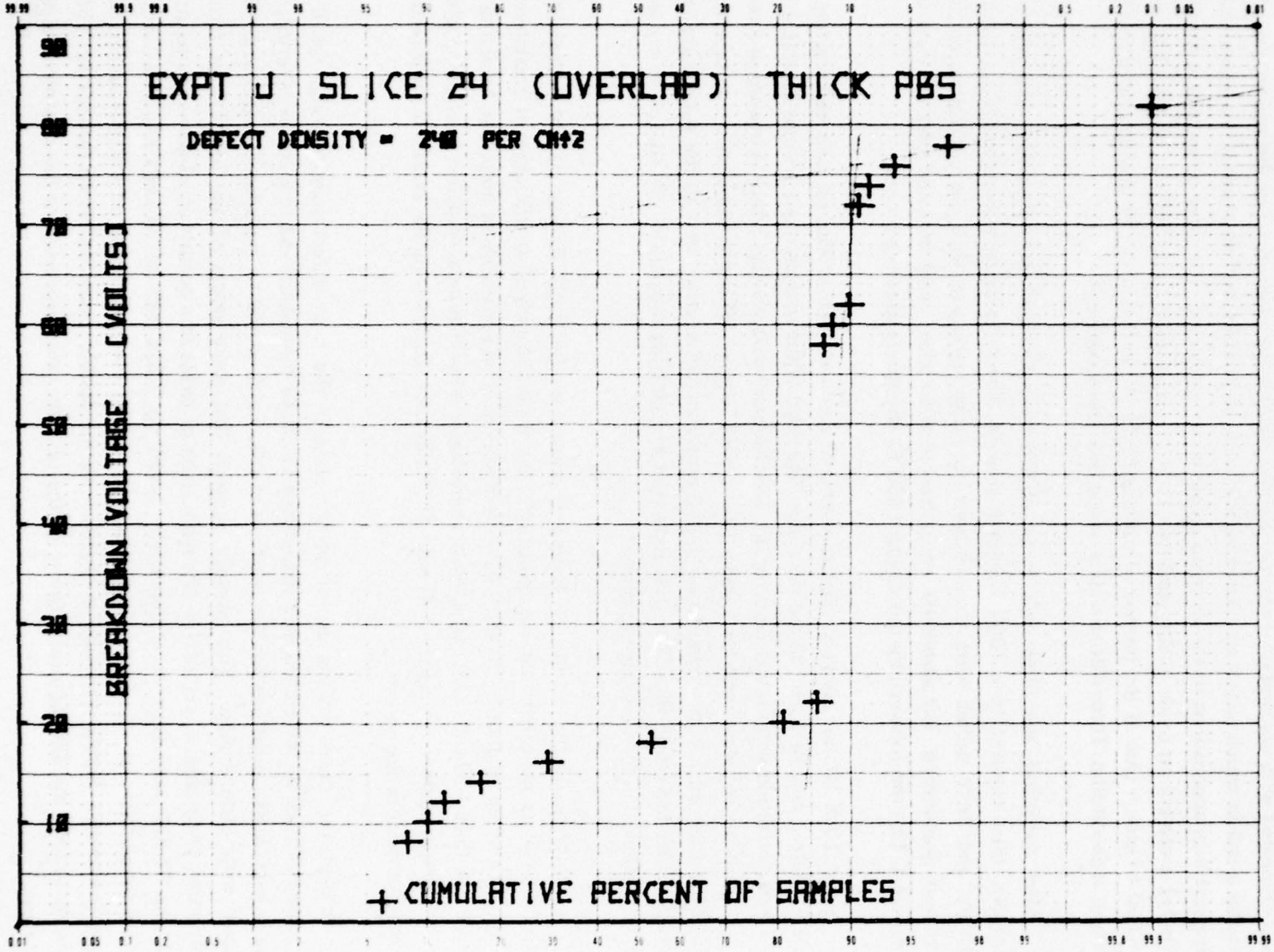


Figure 12. Experiment J: BV Distribution for Overlap Structures Protected with Thick PBS

A question raised in the study of previous data concerned the relative performance of electron resist compared with conventional photoresist processed in the same area. For this reason, this test includes a cell in which wafers are coated with 7500 Å of Hunt PR-104 photoresist, a positive resist comparable in applications to the electron resists being considered. The three other cells in the test included a control on oxide quality and two TI-313 cells, a single coat (5000 Å) and double coat (10,000 Å) group. One of the process advantages of TI-313 is that it can be double coated readily without redissolution. Three silicon wafers were processed in each cell.

After oxidation, the three cells to be etched were coated, baked, developed and rebaked normally, then exposed to a 100% over-etch process. The resist films were removed in organic solvents, and these wafers were cleaned prior to being regrouped with the control wafers for aluminum evaporation. The aluminum was patterned and etched using the same mask array shown in Figure 4. This was followed by the standard 450°C, 50-minute sintering process.

Again, 10 X 10 unit arrays of capacitors of 0.01 cm^2 area were probed on each wafer, giving a total metallized area of 1 cm^2 tested per wafer. The third of the measurement systems described in the Characterization section was used for this test. Negative-going voltage ramps increasing at a rate of −10 volts/second were used for testing these p-type samples. This polarity choice maintains the silicon substrate surface in accumulation during measurement, assuring that all the voltage applied appears across the oxide film. The data reduction and plotting capabilities of this system are the same as that used in the previous experiment.

A summary of the results of testing is shown in Table III. Review of the probability distribution plots indicated that the more defective wafers displayed distributions of breakdown voltage ranging up to about −20 volts. For this reason, data on percentage of units with breakdown voltage less than −20 volts was extracted to characterize gross etch-induced defect level, along with the very low breakdown voltage (−2 V) data. Defect density derived from the extent of the primary breakdown mode is also shown.

Perhaps the most striking aspect of the data is the high defect densities and low-BV percentages for all of the etched material, compared to the control cell and to previous experience. This is particularly surprising for the photoresist cell, which would be expected to withstand this process with little damage. This strongly suggests that some aspect of the handling in resist application, processing, or removal is degrading resist or oxide film quality. In addition, the results with the TI-313 were very wafer dependent: wafer no. 7 had 38% of its units appear as short circuits (conduction at −2 volts or less), while only 1% of the units tested on wafers 8 and 9 had this characteristic. Similar variation is observed on the double-coated wafers 10 through 12. This probably reflects the developmental nature of the electron resist processing of this new material at that time.

Table III. E-Beam Processing
Experiment N: Defect Density Associated with TI-313

Slice No.	Process	Percent Shorted BV ≤ −2 V	Percent of Units with BV ≤ −20 V	Defect Density (cm^{-2})
1	Control	0	0	3
2	Control	0	0	21
3	Control	0	0	18
4	Photoresist Control	0	25	86
5	Photoresist Control	0	25	110
6	Photoresist Control	0	22	138
7	Single Coat TI-313	38	63	240
8	Single Coat TI-313	1	42	299
9	Single Coat TI-313	1	14	97
10	Double Coat TI-313	0	11	139
11	Double Coat TI-313	5	34	265
12	Double Coat TI-313	17	49	281

To obtain the fairest possible comparison of these processes, the probability plot for the wafer with median defect characteristics from each of the four cells is shown in Figures 13 through 16. Overlaying the three latter figures showing data on etched wafers, it is seen that very little difference exists in the shape of the plots. All have a low-voltage distribution including 25% to 40% of the sample below −20 volts, followed by a gradually rising curve to the primary distribution. At the 40-volt level, only 12 percentage points separate the three distributions. While the overall quality is low, it appears the behavior of the TI-313 is not markedly inferior to that of the photoresist, and as mentioned before, is likely related to handling-induced damage.

Characteristics of the two most heavily defective wafers need to be considered in order to understand the nature of the processing problem. Figure 17 is the breakdown data, defect density calculation, and array maps for wafer no. 7, the lowest quality sample in the test. Only 50% of the samples had breakdown voltages above 5 volts. The first array map shows that the greater part of these units lie in the upper left-hand portion of the wafer, while virtually all the units in the lower half of the wafer break down below 5 volts. Locating those units with breakdown voltages above 45 volts confirms this finding, with all but three of these units in the upper left-hand corner in an almost continuous array. This spatial nonuniformity indicates that a problem in resist application or handling is a more likely failure mechanism than inherently poor resist characteristics.

A similar situation is found on wafer no. 12, ranking second in number of low-breakdown units. The array plot in Figure 18 shows that the 24 units with breakdowns below 3 volts lie predominantly in the upper left-hand corner of the wafer.

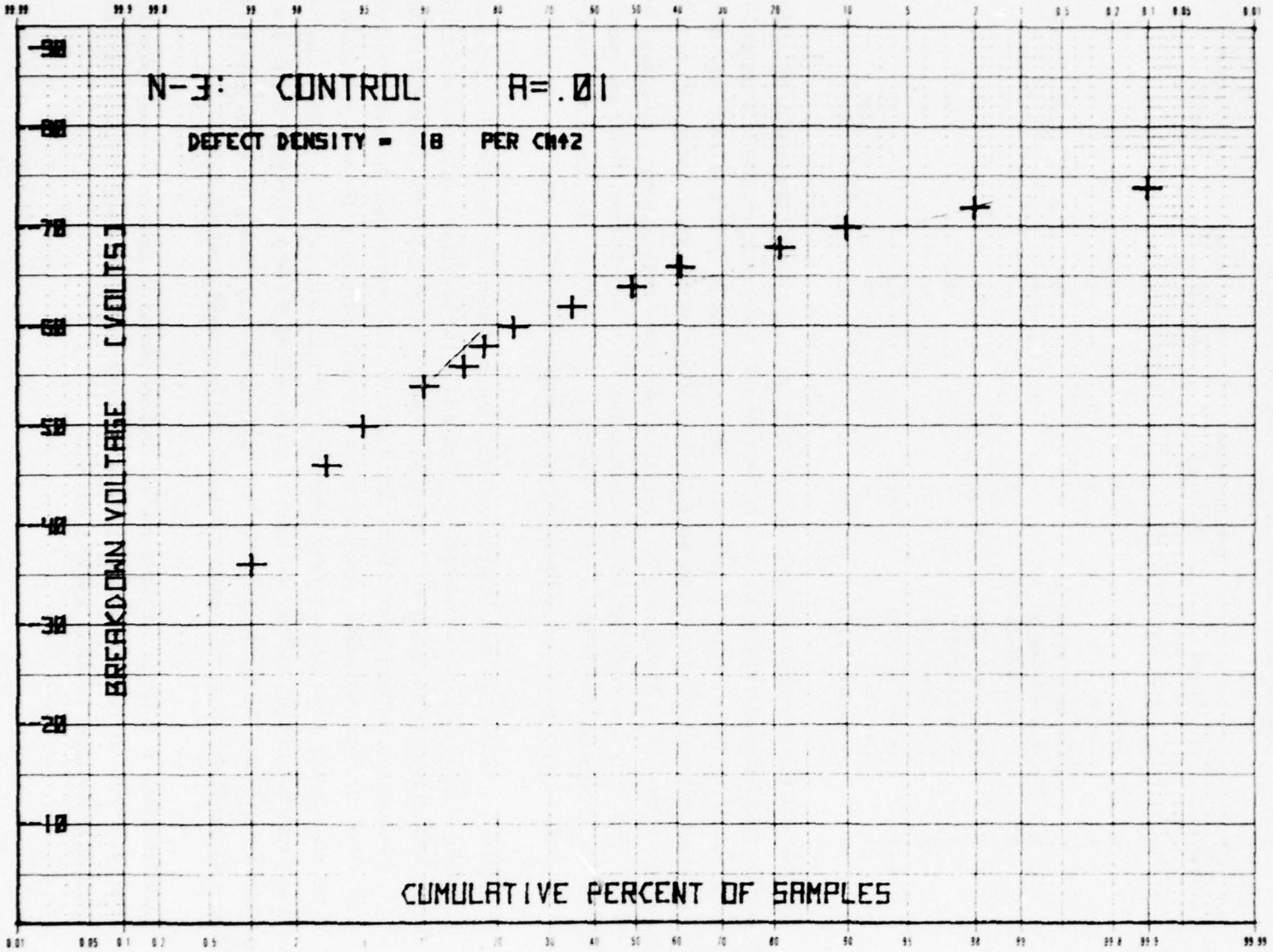


Figure 13. Experiment N: Median BV Distribution for Control Group

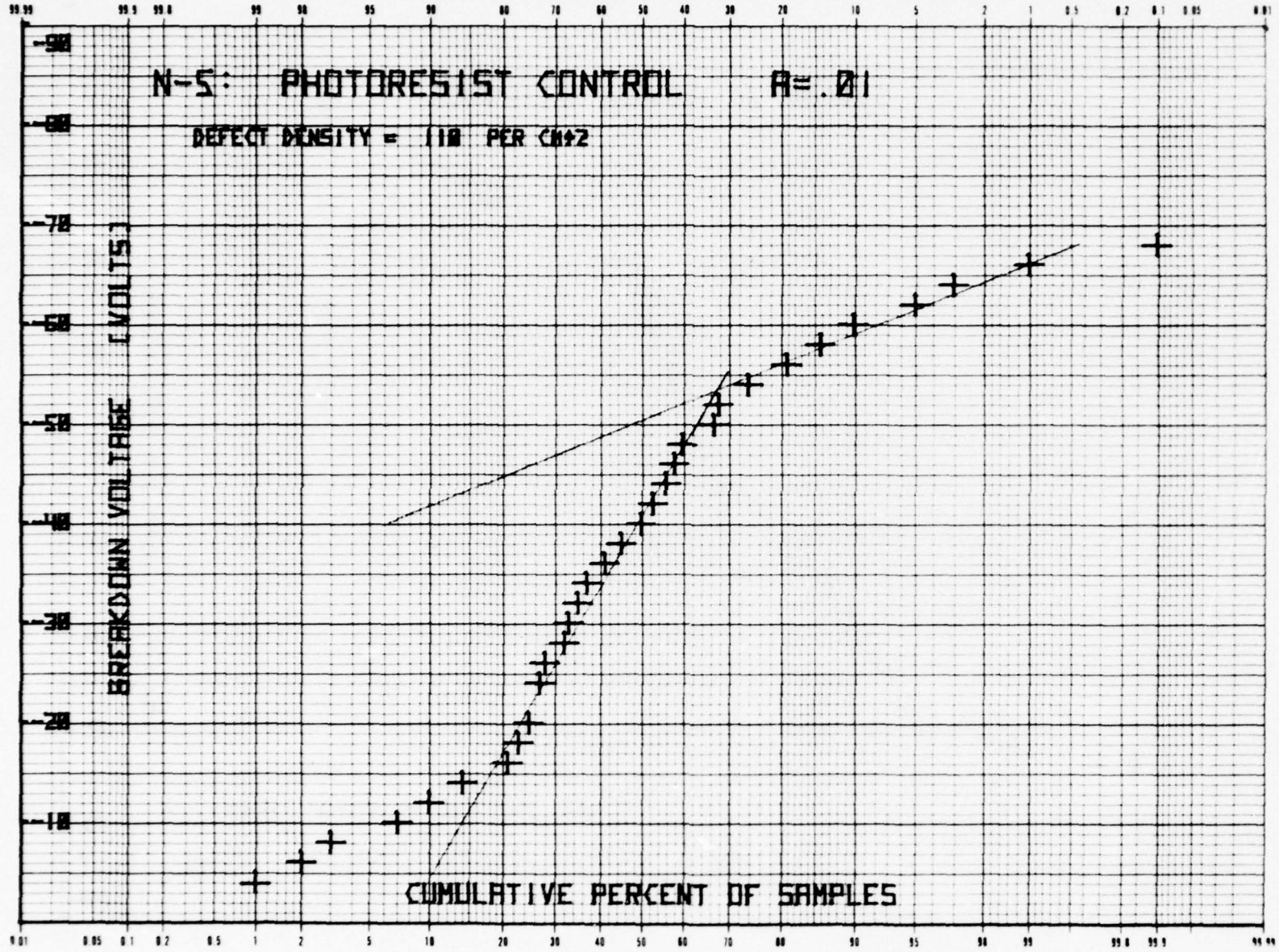


Figure 14. Experiment N: Median BV Distribution for Photoresist Control Group

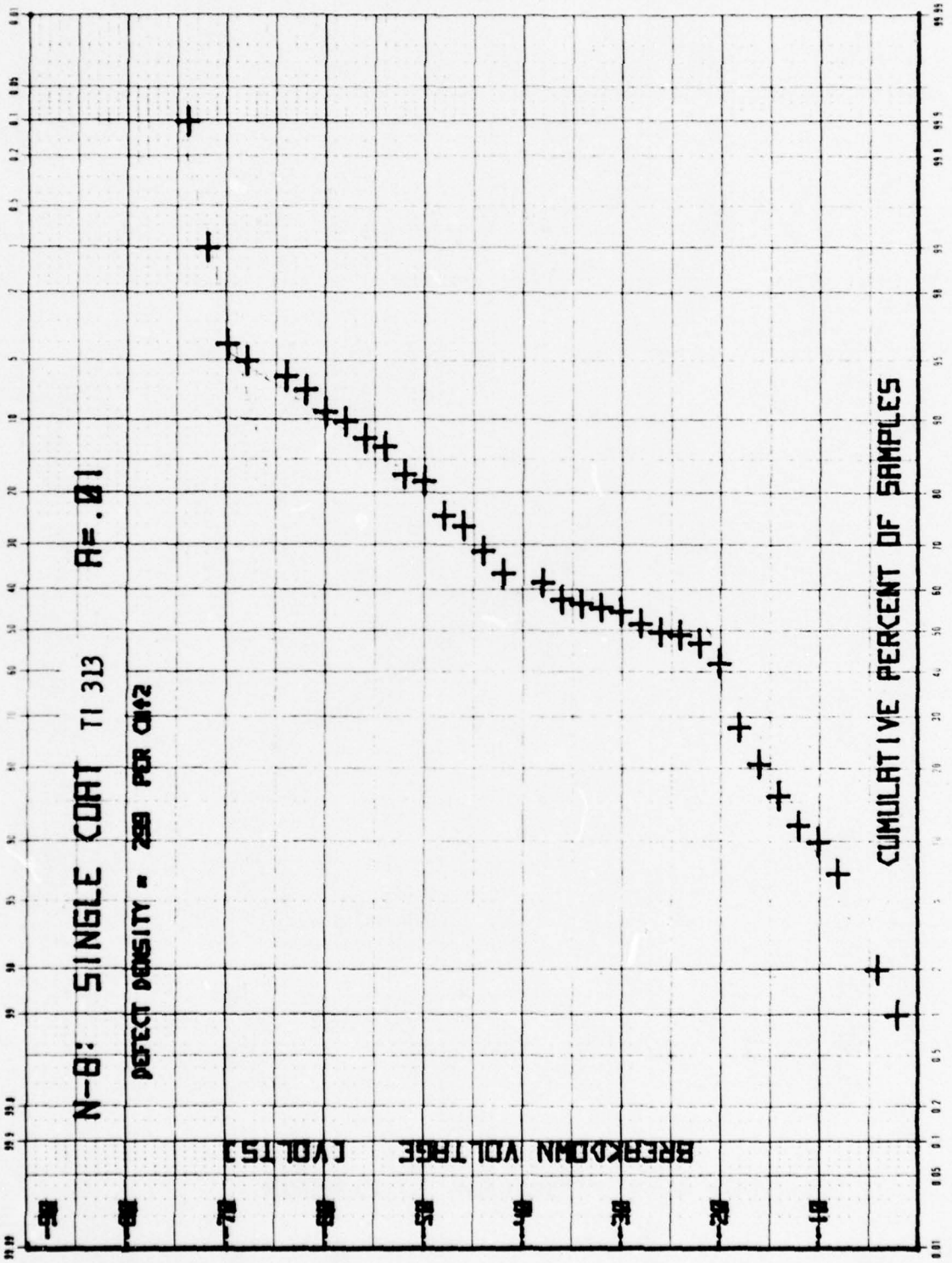


Figure 15. Experiment N: Median BV Distribution for Single Coat TI 313 Group

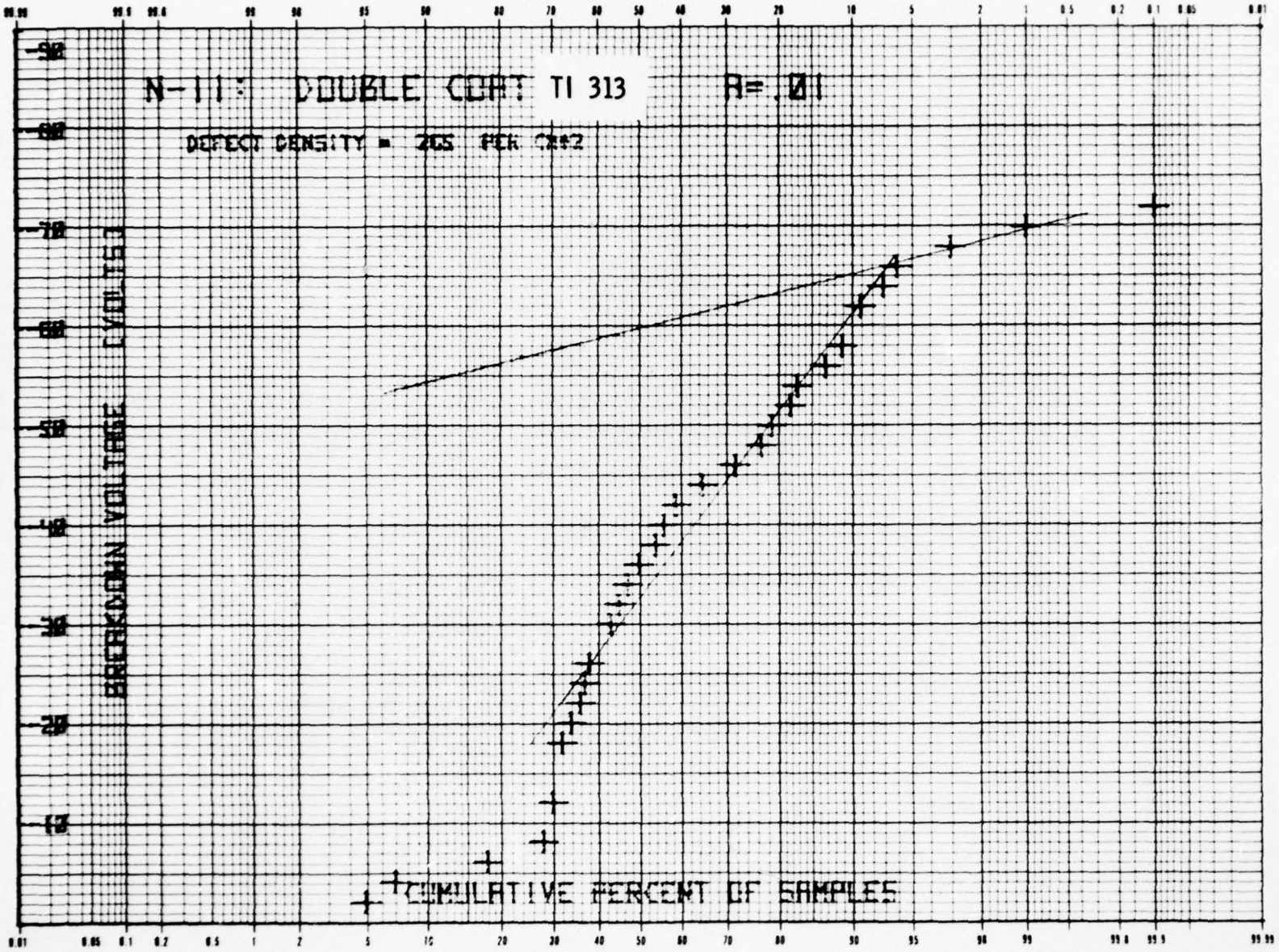


Figure 16. Experiment N: Median BV Distribution for Double Coat TI 313 Group

N-7: SINGLE COAT **TI 313**

RAMP RATE = -10 VOLT/SEC.

CAPACITOR AREA = 0.01 CM↑2 TEST CURRENT = 40 MICROAMP.

VOLTAGE	UNITS IN BREAKDOWN	CUMULATIVE PERCENT
-2.0	38	38.00
-4.0	10	48.00
-6.0	5	53.00
-8.0	2	55.00
-10.0	0	55.00
-12.0	0	55.00
-14.0	2	57.00
-16.0	4	61.00
-18.0	0	61.00
-20.0	2	63.00
-22.0	1	64.00
-24.0	3	67.00
-26.0	4	71.00
-28.0	0	71.00
-30.0	1	72.00
-32.0	2	74.00
-34.0	1	75.00
-36.0	3	78.00
-38.0	1	79.00
-40.0	2	81.00
-42.0	0	81.00
-44.0	1	82.00
-46.0	0	82.00
-48.0	2	84.00
-50.0	1	85.00
-52.0	1	86.00
-54.0	2	88.00
-56.0	1	89.00
-58.0	1	90.00
-60.0	1	91.00
-62.0	0	91.00
-64.0	3	94.00
-66.0	4	98.00
-68.0	0	98.00
-70.0	0	98.00
-72.0	1	99.00
-74.0	0	99.00
-76.0	1	100.00
-78.0	0	100.00
-80.0	0	100.00
-82.0	0	100.00
-84.0	0	100.00
-86.0	0	100.00
-88.0	0	100.00
-90.0	0	100.00
-92.0	0	100.00
-94.0	0	100.00
-96.0	0	100.00
-98.0	0	100.00

TOTAL 100

Figure 17. Experiment N: Breakdown Data, Defect Calculation and Array Map for Lowest Quality Sample (Sheet 1 of 2)

EMAX = -74.69 VOLTS 0.8*EMAX = -59.75 VOLTS

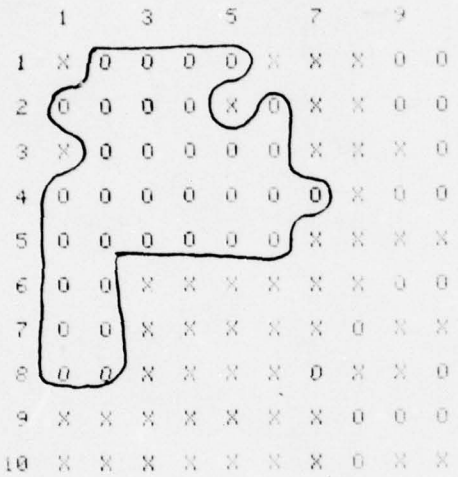
YIELD = 9 PERCENT

DEFECT DENSITY = 240.79 PER SQ. CM.

NUMBER OF OPEN-CIRCUIT DEVICES = 0 (0 PERCENT)

N-7: SINGLE COAT TI 313

X INDICATES BV LESS THAN-5 VOLTS



N-7: SINGLE COAT TI 313

X INDICATES BV LESS THAN-45 VOLTS

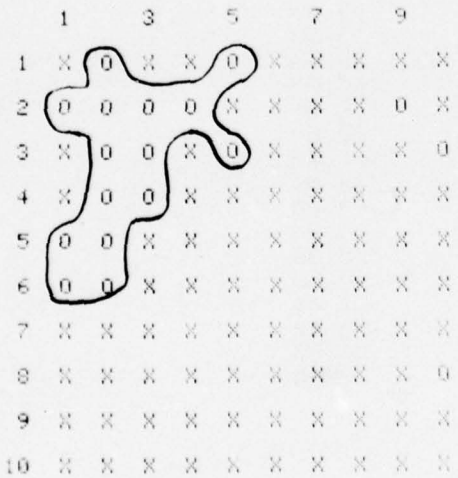


Figure 17. Experiment N: Breakdown Data, Defect Calculation and Array Map for Lowest Quality Sample (Sheet 2 of 2)

N-12: DOUBLE OXAT **TI 313** A=.01

RAMP RATE = -10 VOLT/SEC.

CAPACITOR AREA = 0.01 CM12 TEST CURRENT = 40 MICROAMP.

VOLTAGE	UNITS IN BREAKDOWN	CUMULATIVE PERCENT
-2.0	17	17.00
-4.0	13	30.00
-6.0	6	36.00
-8.0	2	38.00
-10.0	0	38.00
-12.0	2	40.00
-14.0	2	42.00
-16.0	1	43.00
-18.0	3	46.00
-20.0	3	49.00
-22.0	2	51.00
-24.0	3	54.00
-26.0	1	55.00
-28.0	4	59.00
-30.0	4	63.00
-32.0	4	67.00
-34.0	4	71.00
-36.0	5	76.00
-38.0	3	79.00
-40.0	3	82.00
-42.0	2	84.00
-44.0	2	86.00
-46.0	1	87.00
-48.0	1	88.00
-50.0	1	89.00
-52.0	3	92.00
-54.0	1	93.00
-56.0	2	95.00
-58.0	1	96.00
-60.0	1	97.00
-62.0	2	99.00
-64.0	0	99.00
-66.0	0	99.00
-68.0	0	99.00
-70.0	1	100.00
-72.0	0	100.00
-74.0	0	100.00
-76.0	0	100.00
-78.0	0	100.00
-80.0	0	100.00
-82.0	0	100.00
-84.0	0	100.00
-86.0	0	100.00
-88.0	0	100.00
-90.0	0	100.00
-92.0	0	100.00
-94.0	0	100.00

TOTAL 100

Figure 18. Experiment N: Breakdown Data, Defect Calculation and Array Map for the Next-to-Lowest Quality Sample (Sheet 1 of 2)

EMAX = -69.54 VOLTS .8*EMAX = -55.64 VOLTS

YIELD = 5 PERCENT

DEFECT DENSITY = 299.57 PER 80. CM.

NUMBER OF OPEN-CIRCUIT DEVICES = 0 (0 PERCENT)

N-12: DOUBLE COAT TI 313 A=.01

X INDICATES BV LESS THAN-3 VOLTS

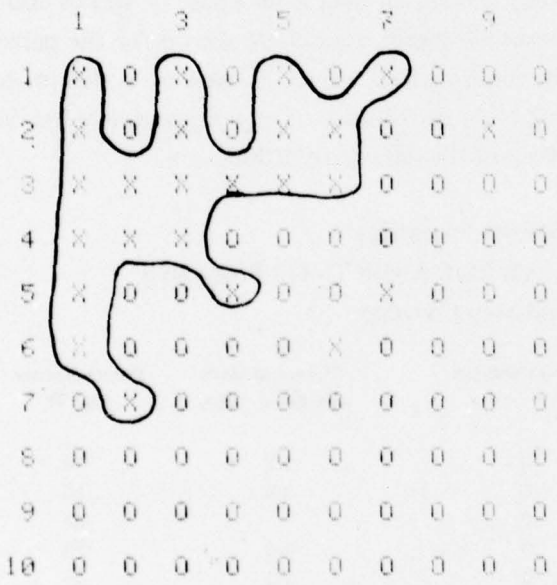


Figure 18. Experiment N: Breakdown Data, Defect Calculation and Array Map for the Next-to-Lowest Quality Sample (Sheet 2 of 2)

In summary, while the overall quality of the results of this test is low, the fact that four of the six TI-313-coated wafers had 5% or less shorted units suggests that there is no inherent problem with resist attack by the etchant, and that circuit fabrication may be feasible. The spatial nonuniformities indicate that more developmental work is needed to make this a production worthy process.

d. EXPERIMENT O: STEP COVERAGE AND HANDLING EFFECTS WITH TI-313

This experiment, done after more work had been completed on TI-313 application, development, and removal, is considerably more sophisticated than the earlier experiment. As before, it includes single and double coat TI-313 as well as Hunt PR-104 photoresist, but controls on wafer cleaning and removal of all three resist films are also present, along with the usual control on as-grown oxide quality. The technique shown in Figure 4 of fabricating nested and overlap capacitors on the same wafer is also employed here. The testing procedure was exactly as described for Experiment N, except that the nested and overlap data from each wafer (100 units each) are plotted on the same probability graph for immediate comparison.

Table IV is a condensed summary of the results, combining the nested and overlap data. With the exception of the four handling control wafers shown, all data is on a base of 400 to 600 units, improving the statistical validity of the comparisons. Again, results are shown for the percent of units shorted and breaking down below some intermediate value, as well as a defect density computed from the extent of the primary breakdown distribution. The voltage ranges for the first two categories were chosen on the basis of a survey of the data distributions.

Table IV. E-Beam Processing
Experiment O: Defect Density Associated with TI-313 Processing
Periphery and Step Coverage

Slice No.	Process	Percent Shorted BV < −10 V	Percent of Units with BV ≤ −40 V	Defect Density (cm^{-2})
0-1, 3	Control	0.5	1.7	26
0-4	Control – No Etch	0	0.5	50
0-8	Photoresist – No Etch	0	0	84
0-12	Single TI-313 – No Etch	0	3.0	39
0-16	Double TI-313 – No Etch	0	3.3	25
0-5, 7	Hunt PR-104	0.75	1.5	83
0-9, 11	Single Coat TI-313	1.7	6.3	65
0-13, 15	Double Coat TI-313	0.25	3.0	76

The quality of the results is considerably improved over the first test done with TI-313. Defect densities are all well below 100/cm^2 and the overall percentage of shorted units for the worst cell is less than 2%. In that regard, the percentage of shorted units follows the thickness of the resist film, from single-coat (5000 Å) TI-313 through PR-104 to double-coat TI-313 (10,000 Å) without dependence upon resist type.

The resist removal control wafers 0-8, 12, and 16 indicate that a problem still exists in damaging oxides in the removal of TI-313. The percentage of units breaking down below −40 volts is significantly higher than the control, and this effect is again noted in the etched-wafer data. Inspection of the probability distributions suggests that much of the rounding of the curves just below the primary distribution is induced by handling and cleaning of the resist-coated wafers. Still, the improved techniques implemented in the interim between Experiment N and O have significantly reduced the level of this problem.

Another encouraging aspect of this test is seen in Table V, where a more detailed listing of the data is shown separating the nested and overlap capacitor results. In no case is there a significantly greater percentage of shorted units on overlap arrays than on the corresponding nested arrays on the same wafer. This is strong evidence that step coverage is well in hand with this resist and associated process technology.

Table V. Experiment O: Defect Density Associated with TI-313 Processing Periphery and Step Coverage

		BV < −10 V (%)		BV < −40 V (%)		Defect Density (cm^{-2})	
Slice No.	Sample Description	Nested	Overlap	Nested	Overlap	Nested	Overlap
0-1	Control	1	1	4	2	18	17
0-2	Control	0	0	0	0	23	17
0-3	Control	0	1	0	2	34	46
0-4	Control – No Etch	0	0	1	0	38	61
0-8	Hunt PR – No Etch	0	0	0	0	86	82
0-12	Single TI-313 – No Etch	0	0	4	2	40	38
0-16	Double TI-313 – No Etch	0	0	4	2	23	27
0-5	Hunt PR-104	2	1	2	1	91	104
0-6	Hunt PR-104	–	–	–	–	–	–
0-7	Hunt PR-104	0	0	3	0	69	69
0-9	Single Coat TI-313	4	3	9	6	53	52
0-10	Single Coat TI-313	1	0	4	8	37	51
0-11	Single Coat TI-313	1	1	8	3	96	102
0-13	Double Coat TI-313	0	0	0	6	31	56
0-14	Double Coat TI-313	0	1	5	1	120	96
0-15	Double Coat TI-313	–	–	–	–	–	–

A group of six probability plots from various wafers in each of the cells of the test is shown in Figures 19-24 to permit a more detailed comparison of results. Overlaying the entire group shows relatively little dependence on resist or processing, particularly compared to the early tests with the PBS that yielded such poor device fabrication results. Based upon these findings and the continuously developing process technology, it appears safe to conclude that a reasonable yield of relatively complex integrated circuits should be obtainable in the immediate future using e-beam technology in conjunction with TI-313 electron resist.

3. Conclusions

Conclusions to be drawn from the above work have been discussed separately with regard to each of the different tests. Two overall statements can be made, however. First, correlation of the nature and density of the defects found on integrated circuits fabricated using PBS with short-circuit data found on MOS capacitor test wafers having stepped oxides indicates that the failure of the PBS during oxide etching was the predominant cause of low functional circuit yields. This has been confirmed by the isolation and identification of oxide pinholes on circuit wafers using optical and scanning electron microscopy. For example, Figure 25 is a scanning electron micrograph of a partially-etched-through pinhole in a deposited oxide multilevel insulator film. The small hole at the bottom of the crater is probably the site of an electrostatic discharge failure between an upper aluminum electrode (which has been removed) and the silicon substrate. The view at lower magnification in Figure 26 shows the location of the pinhole in the middle of an interdigitated array. The square darkened area is the result of oxide surface charging which occurred during the making of Figure 25. Other smaller defect sites are visible above and to the far left of the first pinhole. The severe damage at the top of Figure 26 is an artifact of the sample preparation for study and is not related to electron resist failure. The association of the pinholes shown here with electron resist failure is based upon the high incidence of electrical shorts of test structures like this which were fabricated with electron beam processing compared to companion structures built with standard photolithographic techniques. Analysis of the shorted units revealed defect sites such as the one shown in Figures 25 and 26. Figures 27(a-e) show optical photomicrographs of other pinholes found on circuits and test structures fabricated with PBS electron resist.

The second group of experiments permits us to conclude that the TI-313 electron resist and associated processing gives significantly better results in continuity and step coverage, being comparable to commercially available photoresist. This technology should permit fabrication of complex integrated circuits at reasonable yield in the immediate future.

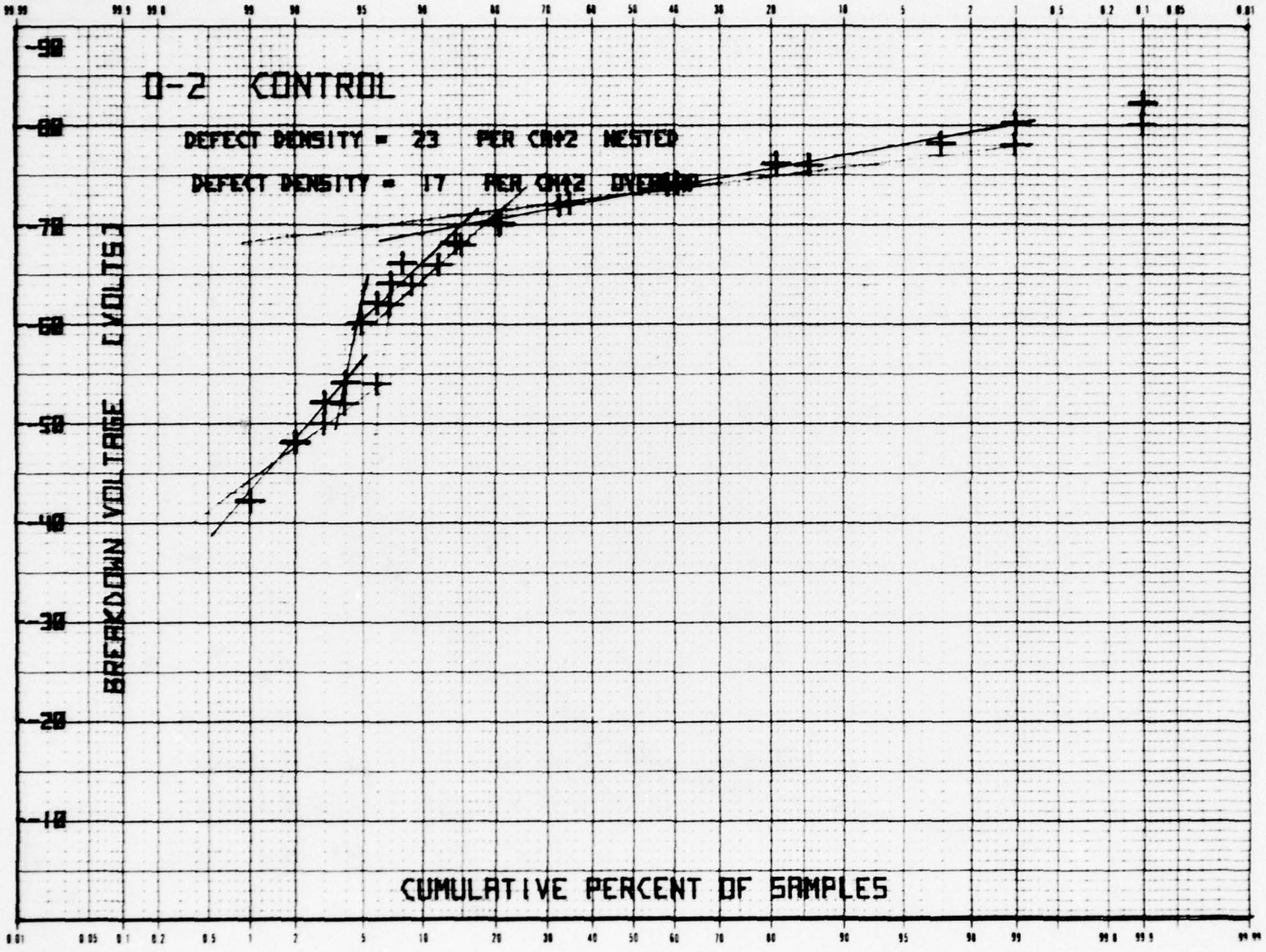


Figure 19. Experiment O: Typical Control Group BV Distribution (Nested and Overlap)

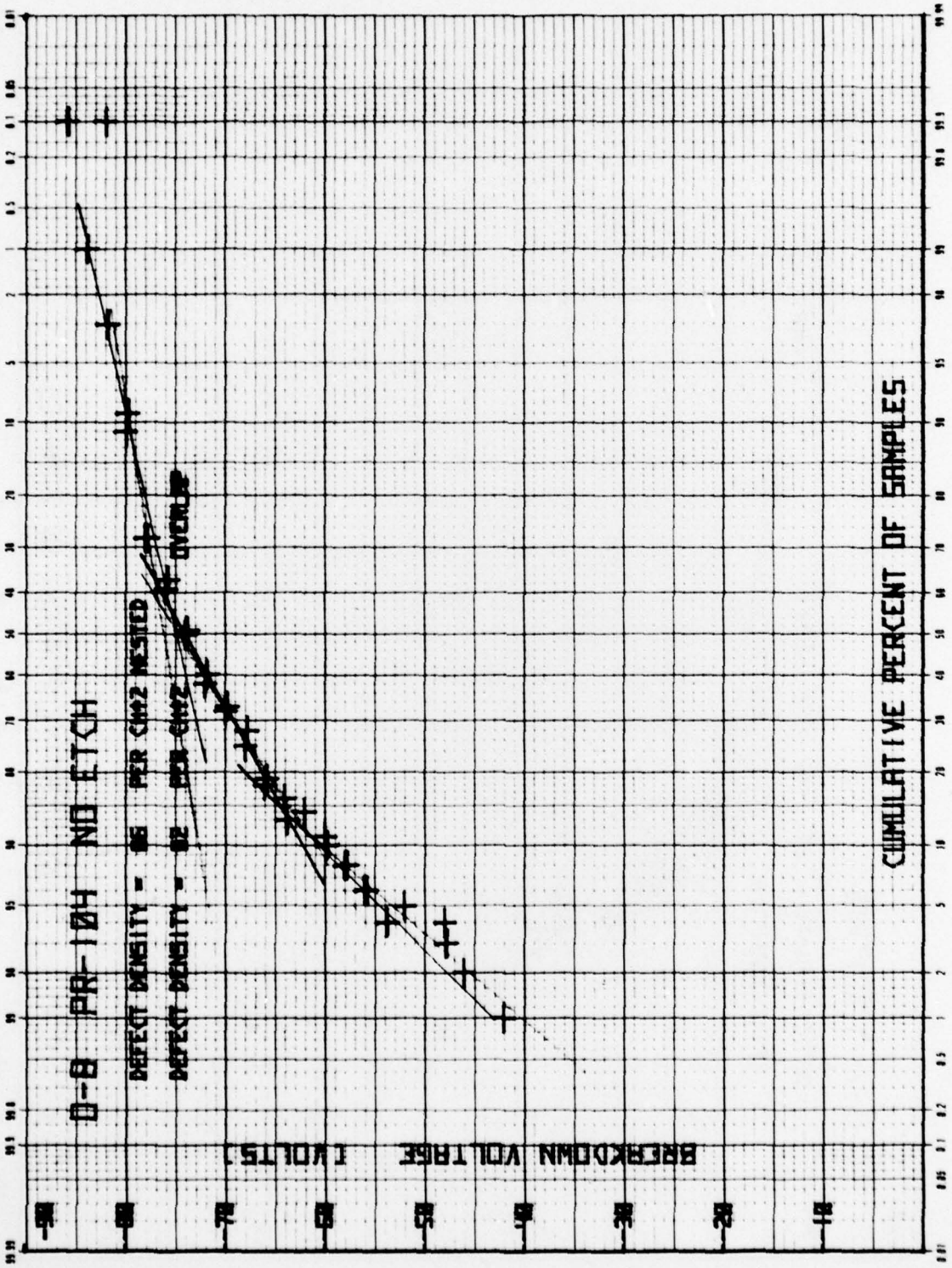


Figure 20. Experiment O: Typical BV Distribution from the PR-104/No Etch Group (Nested and Overlap)

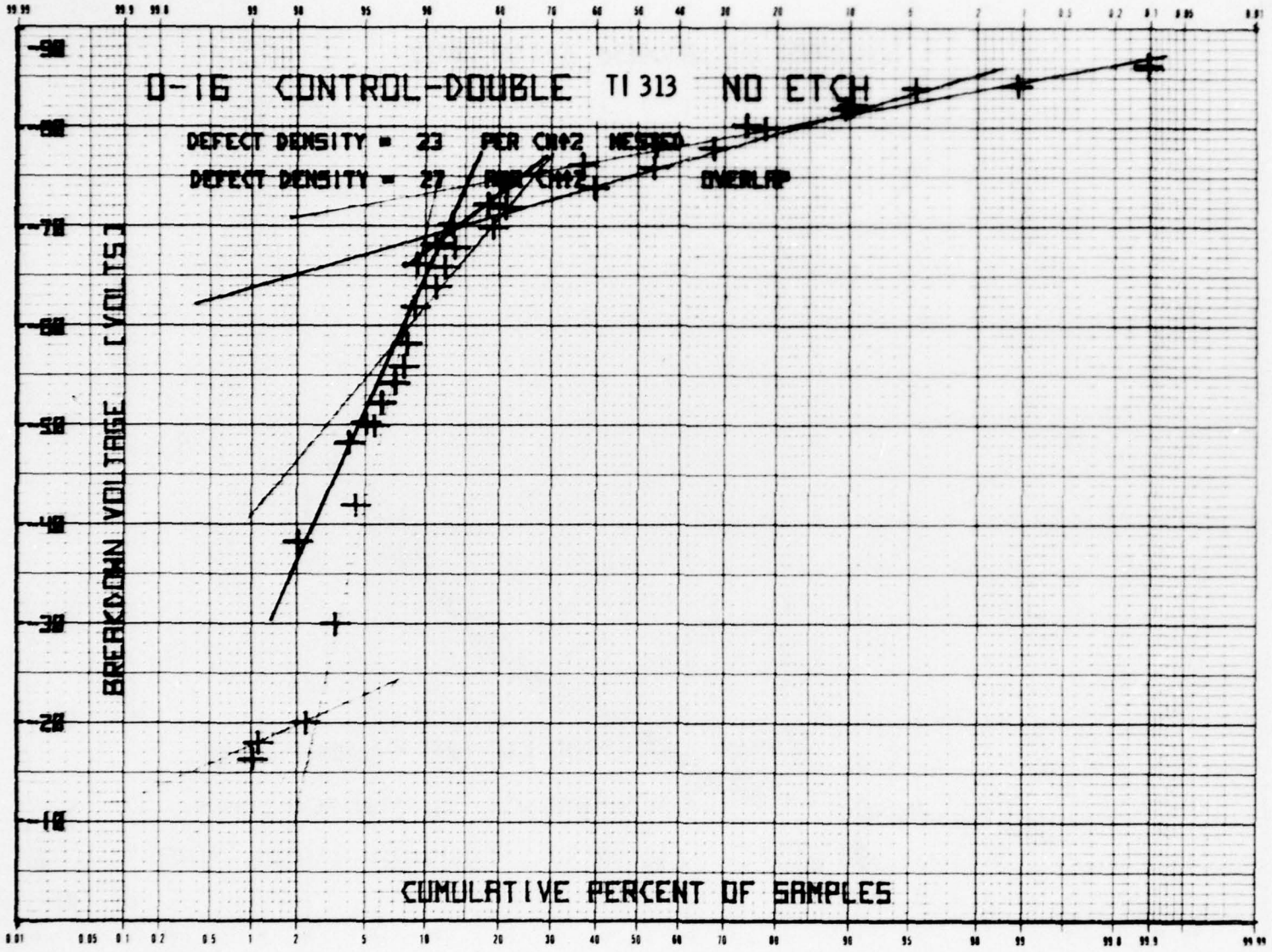


Figure 21. Experiment O: Typical BV Distribution from the Double-Coated TI 313/No Etch Control Group

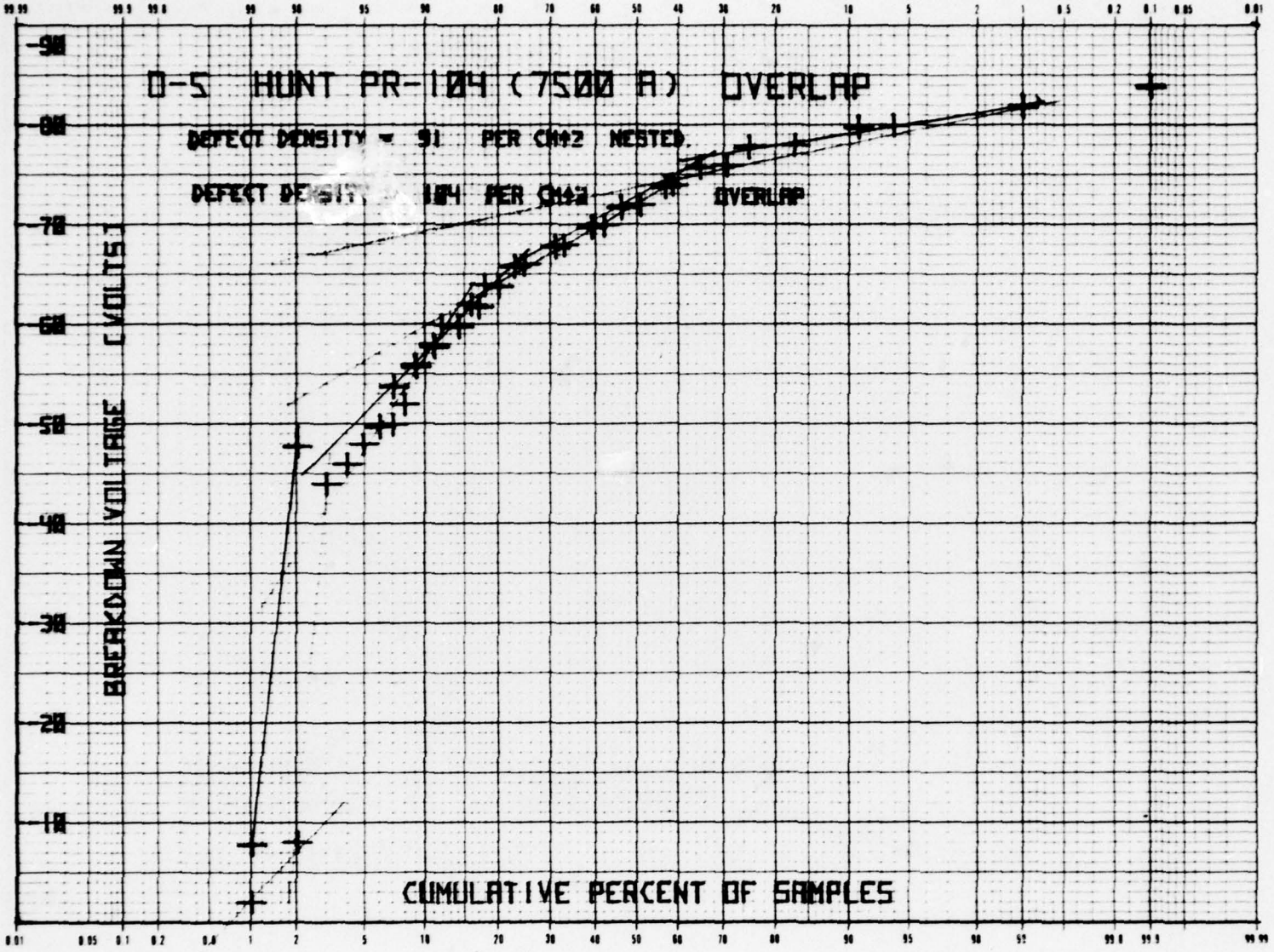


Figure 22. Experiment O: Typical BV Distribution from PR-104/Etched Group (Nested and Overlap)

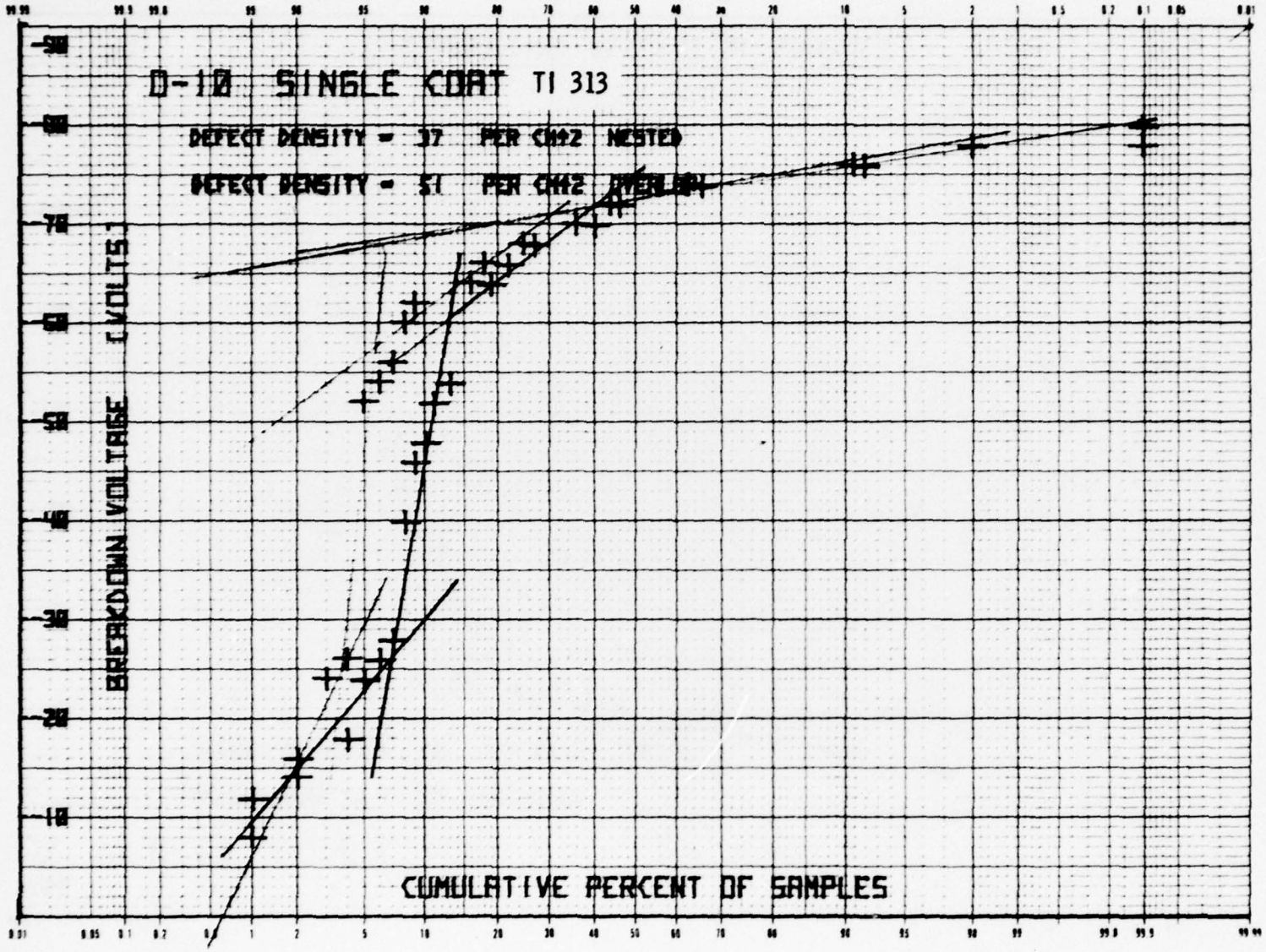


Figure 23. Experiment O: Typical BV Distribution from the Single Coat TI 313/Etched Group (Nested and Overlap)

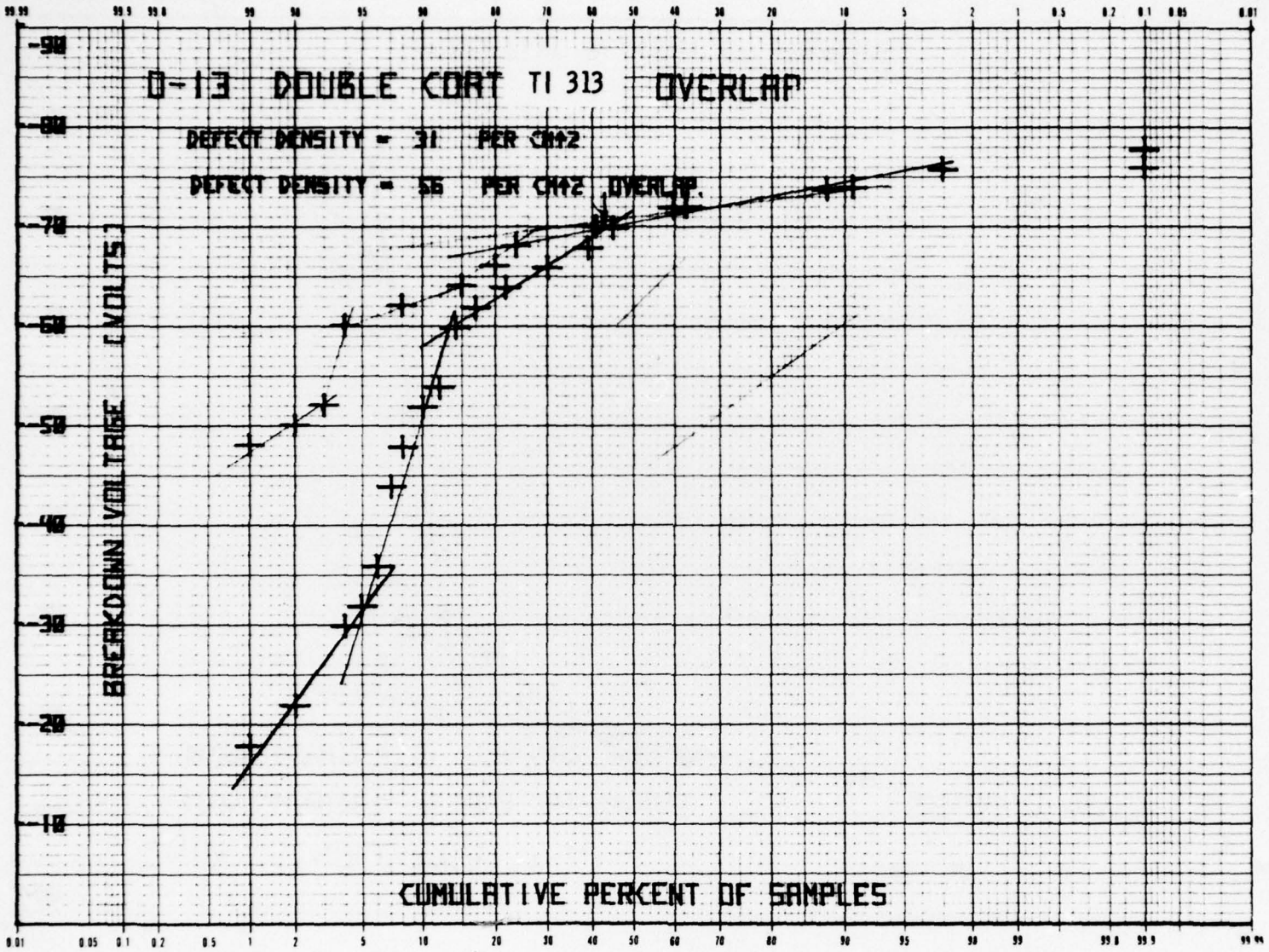
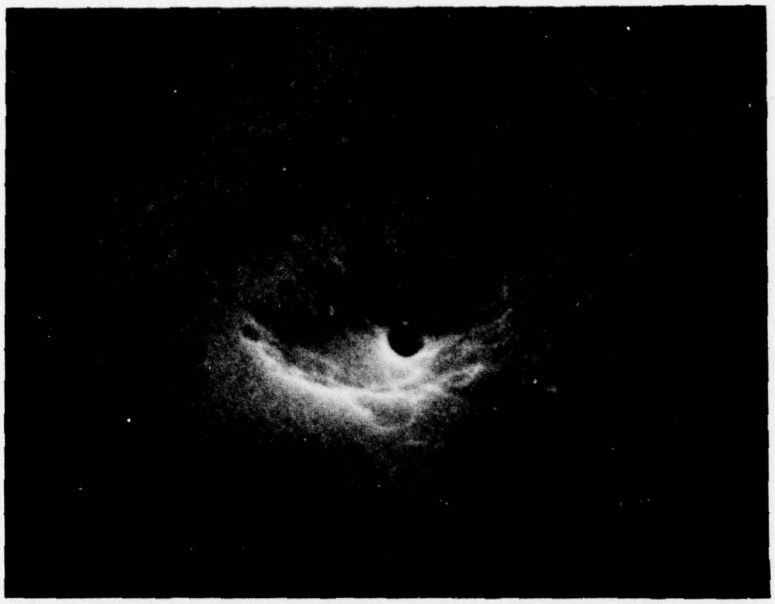
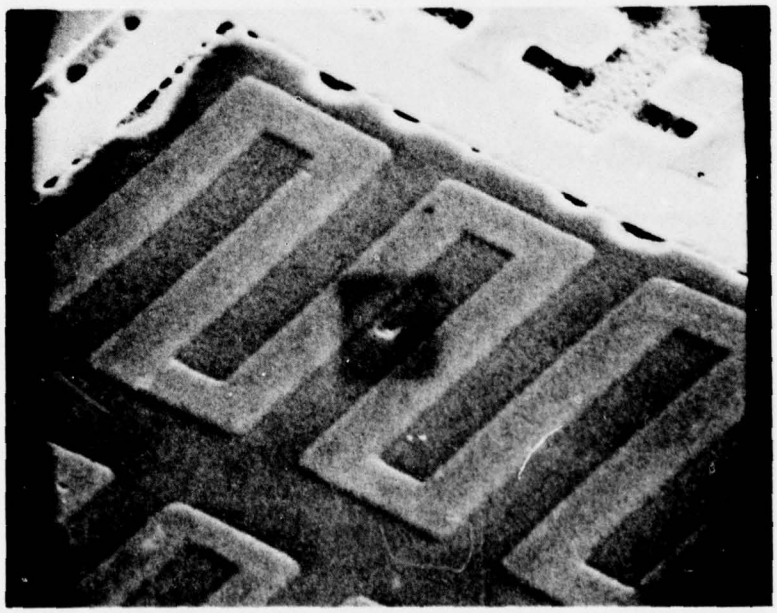


Figure 24. Experiment O: Typical BV Distribution from the Double Coat TI 313/Etched Group (Nested and Overlap)



10,000X, 60°

Figure 25. Scanning Electron Micrograph of a Pinhole Defect Site



1,000X, 60°

Figure 26. Scanning Electron Micrograph Array Containing Defect Shown in Figure 25

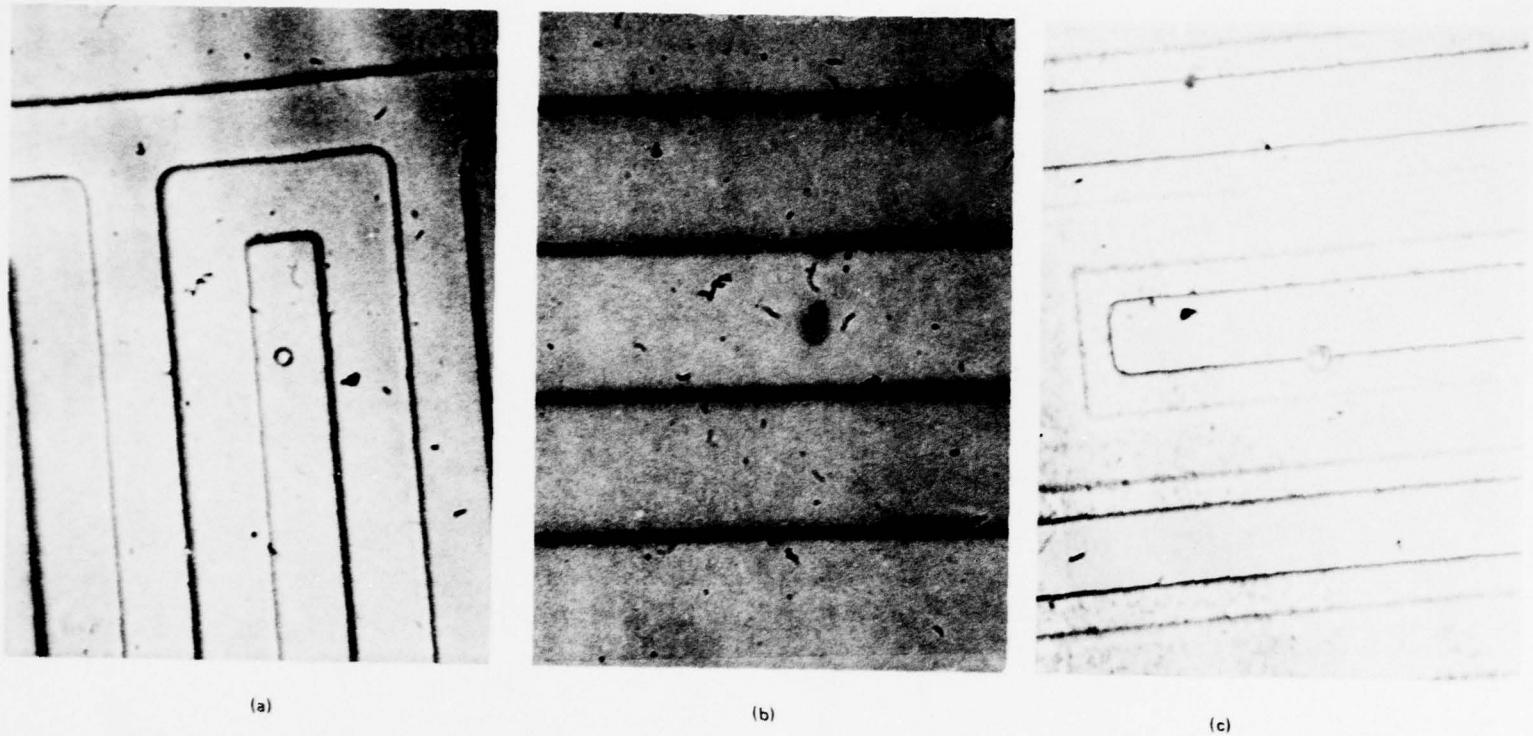
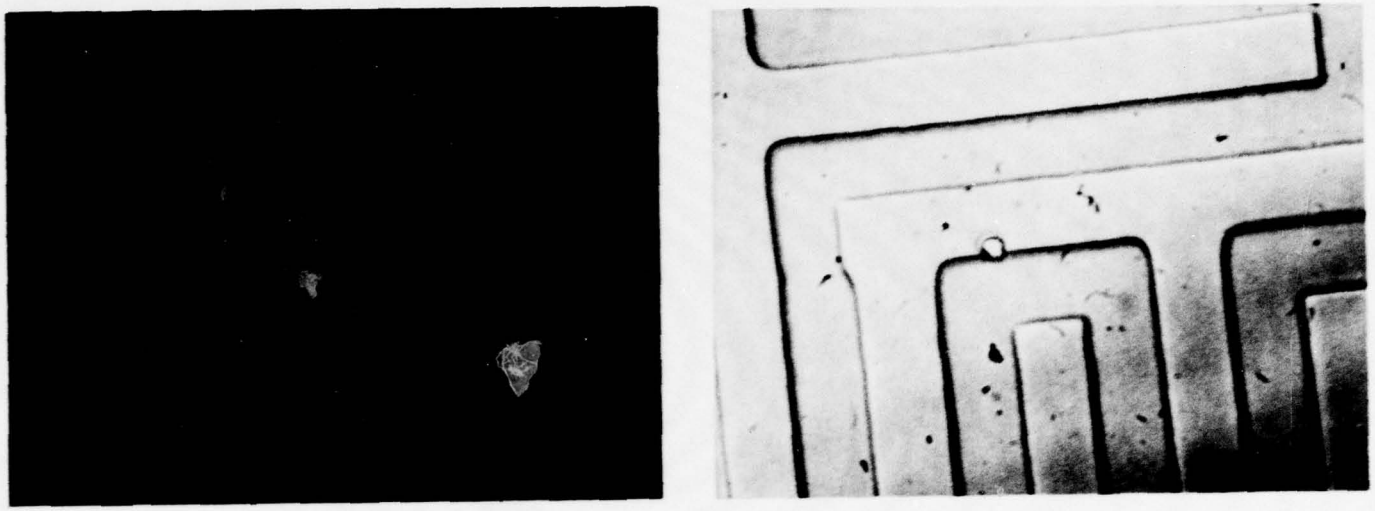


Figure 27. Optical Photomicrographs of Pinholes in PBS-Fabricated Microcircuits (Sheet 1 of 2)



(d)

(e)

Figure 27. Optical Photomicrographs of Pinholes in PBS-Fabricated Microcircuits (Sheet 2 of 2)

SECTION III
MANPOWER

The following professionals worked on this program from 1 September 1977 to 1 December 1977. The hours worked are shown.

Mr. P. L. Whelan	30
Mr. R. A. Williamson	585
Dr. G. L. Varnell	60
Dr. J. L. Bartelt	60
Dr. T. L. Brewer	Consultant
Mr. G. A. Brown	60
Dr. R. A. Robbins	Consultant
Mr. C. D. Winborn	Consultant

In addition, three technicians worked on the program.